Transmission electron microscopy study of $In_{0.83}Ga_{0.17}As$ photodetectors with linearly graded $In_xAl_{1-x}As$ buffer and digital graded superlattices

LIANG ZHAO[a], ZUOXING GUO[a], LI LIU[a], XINGYOU CHEN[b], YI GU[b], LEI ZHAO[a,*]

[a]*Key Lab of Automobile Materials, Ministry of Education, College of Materials Science and Engineering, Jilin University, Nanling Campus, Changchun, 130025, P.R. China*

[b]*State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai, 200050, P.R. China*

InGaAs photodetector with linearly graded $In_xAl_{1-x}As$ buffer and digital graded superlattices (DGSLs) was studied by high-resolution transmission electron microscopy (HRTEM). The upgrade of the properties of photodetector has been verified in structure. Linearly graded $In_xAl_{1-x}As$ buffer layer effectively restrained the motion of threading dislocations (TDs). The cross-section high-resolution images proved the digital graded superlattice markedly decreased the TDs density in absorption layer. Furthermore, the DGSL structures reduced the conduction band discontinuity in heterojunction interface.

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1. Introduction

$In_{0.83}Ga_{0.17}As$ photodetectors (PDs) with the cut-off wavelength of 2.5 μm attracted more interests in recent years [1, 2]. InGaAs PDs were often fabricated on InP substrates [3]. Lattice mismatch of ~2% between $In_{0.83}Ga_{0.17}As$ and InP substrate brings about epilayer amount of stress. The progress of stress relaxation is usually determined by the formation of dislocations which will degrade the performance of the detectors [4, 5]. To reduce the dislocation density and improve the material quality several different buffer layers have been implemented between the InP substrate and the $In_{0.83}Ga_{0.17}As$ absorption layer, e.g., using a thick uniform buffer layer [6], a step-graded buffer layer [7], and a linearly graded buffer layer [8]. Recently, digital graded superlattice (DGSL) was also employed to restrain threading dislocations (TDs) [9]. Due to the high band gap offset and lattice mismatch between the $In_xAl_{1-x}As$ buffer or cap layer and $In_yGa_{1-y}As$ absorption layer, electric charge accumulation and band sharp peak would be generated in the heterogeneous interface [10], which affects the performance of the PDs.

In earlier papers, $In_yGa_{1-y}As$ PDs with linearly graded $In_xAl_{1-x}As$ buffer and DGSL have been studied [11, 12]. Results show that the dark currents are dominated by diffusion current in the vicinity of zero bias. With the increase of reverse bias, recombination current and ohmic current play an increasing leading role. The DGSLs adopted at the InAlAs/InGaAs hetero-interfaces and the initiative InP buffer layer are effective for improving the dark current characteristic. However, the mechanism of performance optimization by this structural design has not been analyzed and discussed deeply. In this work, we introduced DGSL layers into a graded buffer. The insertion of two DGSL layers intermediately into an InAlAs/InGaAs heterogeneous interface was reported, and the distinct effects on the PDs performance of the DGSL intermediate layers have been validated. The transmission electron microscopy (TEM) and high-resolution transmission electron microscopy (HRTEM) were used to analyze the structure of the PDs and the upgrade of the properties of PD has been verified in structure.

2. Material and methods

The growth was performed in a VG Semicon V80H gas source MBE system. The best background chamber pressure achieved in this system was about 1×10^{-11} Torr. The elemental indium, gallium, and aluminum sources were used as group III sources, and their fluxes were controlled by changing the cell temperatures. Arsine and phosphine cracking cells were used as group V sources, and their fluxes were controlled by adjusting the pressure. The cracking temperature was approximately 1000 ºC measured by using a thermocouple. Standard Be and Si effusion cells were used as p- and n-type doping sources, and the doping levels were also controlled by changing the temperatures of cells. The chamber pressure during the growth was about 5×10^{-5} Torr. The samples were grown on N^+ (100) InP epi-ready substrates and started with an InP buffer layer grown at 510 ºC, and then the substrate temperature was decreased to 440 ºC for the following growth. The $In_{0.52}Al_{0.48}As$ buffer was then prepared followed with a composition graded $In_xAl_{1-x}As$ layer

where the indium composition x was designed grading from 0.52 to 0.83 through the simultaneous increase in indium source temperature and decrease in aluminum source. After that, the growth temperature was kept at 470 ºC for following layers, i.e. a N^+ $In_{0.83}Ga_{0.17}As$ template, a n^- $In_{0.83}Ga_{0.17}As$ absorption layer sandwiched between two n^- $In_{0.83}Ga_{0.17}As/In_{0.83}Al_{0.17}As$ DGSL layers and a P^+ $In_{0.83}Al_{0.17}As$ cap layer [11].

After growth, the structure of the PD sample was observed by transmission electron microscopy (TEM, JEM-2100F, JEOL) with Energy dispersive X-ray spectroscopy (EDS, IET250, OXFORD). High resolution transmission electron microscopy (HRTEM) was used for [110] cross-section sample in order to determine the variation of the structure of linearly graded $In_xAl_{1-x}As$ buffer and DGSL along the growth direction. The cross-section sample was prepared by focused ion beam (FIB, FEI Quanta 3D FEG).

3. Results and discussions

Fig. 1 shows the TEM bright-field image with EDS analysis and schematic structure of the sample. It is obvious that in linearly graded $In_xAl_{1-x}As$ buffer layer, most misfit dislocations (MDs) are localized at the interface, after the $In_{0.83}Ga_{0.17}As$ template the DGSL-1 structure showed dark pattern and was free of dislocations. From the EDS spectra the regions of layers in PD were clearly shown. Finally, the dislocation density is significantly reduced in the absorption layer, with the density estimated to be less than 10^8 cm^{-2}. In order to investigate the dislocations structure thoroughly, the linearly graded $In_xAl_{1-x}As$ buffer and DGSL layers were analyzed as follows.

In order to investigate the dislocations' structure thoroughly, the linearly graded $In_xAl_{1-x}As$ buffer and DGSL layers were analyzed by TEM and HRTEM. Fig. 2 shows the [110] cross-section images of the linearly graded buffer layer. From the Fig. 2(a) it could be seen that a number of dislocations are generated in the graded buffer due to the lattice mismatch. Fig. 2(b) shows the HRTEM of a typical misfit dislocation in graded buffer, the magnified Inverse Fast Fourier Transform (IFFT) of green frame area is shown in right. Extra half-planes of atoms are found to be along the (1-11) plane (signed by white "T"), The projections of the total Burgers vectors of the defect complexes on the image plane are determined by constructing Burgers circuits [13] around the defect regions in the HRTEM images, Burgers vector analysis indicates that the projection of the Burgers vector b is *a/2<110>*, parallel to the interface. The misfit dislocation at the linearly graded buffer layer is a perfect 60° dislocation and it has been realized that the most of misfit dislocations at graded buffer layer are 60° dislocations. The strain comes from the lattice mismatch is released efficiently in the linearly graded $In_xAl_{1-x}As$ buffer layer, and the reactions between the dislocations in the heterojunction interfaces restrained the TDs' formations, so the dislocation density in the layer next to the buffer was decreased obviously.

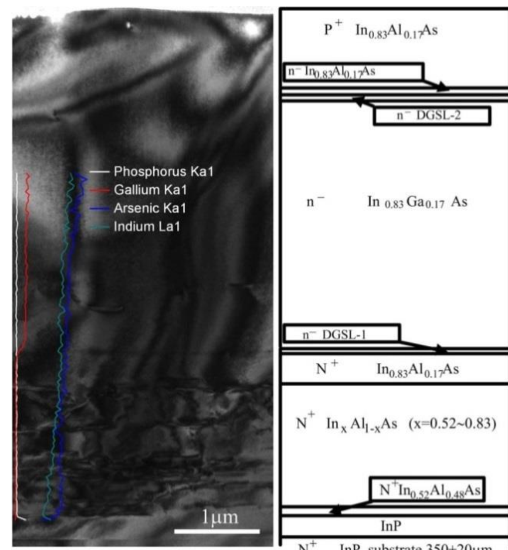

Fig. 1. Cross-section TEM image with EDS and schematic structure of the InGaAs PDs

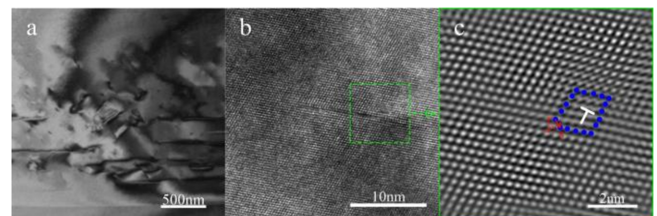

Fig. 2. The TEM image of In content graded $In_xAl_{1-x}As$ (x=0.52~0.83) buffer layer (g=1-11) (a), HRTEM image of typical dislocations structure in buffer layer (cross-section sample, axis zone [110]) (b) and IFFT partial enlargement image (green square in (b)) (c)

The DGSL layer is formed by nine periods ~100 Å superlattice unit cells. Each superlattice unit cell in DGSL-1 layer has a combination of different well/barrier ($In_{0.83}Ga_{0.17}As$/ $In_{0.83}Al_{0.17}As$) thickness ratio (1:9, 2:8, 3:7, 4:6, 5:5, 6:4, 7:3, 8:2, 9:1). Each superlattice unit cell in DGSL-2 layer has a combination of different well/barrier ($In_{0.83}Ga_{0.17}As$/ $In_{0.83}Al_{0.17}As$) thickness ratio (9:1, 8:2, 7:3, 6:4, 5:5, 4:6, 3:7, 2:8, 1:9). Fig. 3(a) shows the TEM image of the structure of DGSL-1 and the HRTEM image of partial enlargement of superlattice. Yellow lines in Fig. 3(a) show the schematic conduction band diagrams at zero bias for DGSL-1. The dotted lines denote the effective barrier height for each superlattice unit cell, which can create a staircase-like barrier in the DGSL layer. The intersubband transitions from the ground bound state, E1, to the E9, E10, and E11 excite states contribute to the broadband detection under positive bias condition, while only transition from the E1 to E11 state is observed under negative bias condition because the photogenerated carriers need to surmount the high abrupt side of the barrier layers [14]. The conduction band discontinuity in heterojunction interface has been decreased.

Fig. 3(b) shows the HRTEM image of red frame area of Fig. 3(a). It has been measured the d(111) of $In_{0.83}Ga_{0.17}As/In_{0.83}Al_{0.17}As$ are measured as 3.458 Å and

3.459 Å, respectively. From the measurement results, the constants have been calculated to be a_1= 5.9895 Å and a_2=5.9908 Å. The value of the lattice mismatch f can be calculated to be 0.0216 %, which is too small to be considered. One defect has been found in DGSL layer (Fig. 4(a)). The region with the SF is magnified from the blue frame in Fig. 4(a), as shown in Fig. 4(b). A 90º partial dislocation and a 30º partial dislocation are located at the two ends of the SF. MD simulations shows that an extended 60º dislocation will constrict and form a full dislocation when its motion on the plane is restrained [15, 16]. The extended 60º dislocation is consist of a 30º leading partial dislocation, a 90º trailing partial dislocation and a short SF between the two partial dislocations. By means of above the results the TD density in the $In_{0.83}Ga_{0.17}As$ absorption layer was decreased obviously.

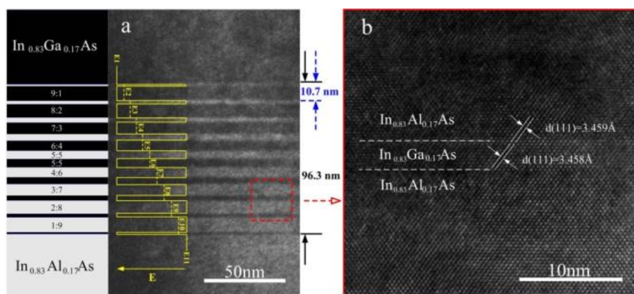

Fig. 3. The TEM image showing the $In_{0.83}Ga_{0.17}As$ medium dark and $In_{0.83}Al_{0.17}As$ bright layers in the DGSL-1 structures (a) and HRTEM image of partial enlargement of superlattice (red square in (a)) (b)

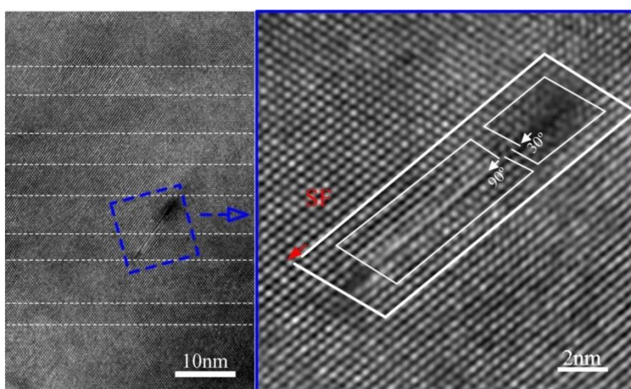

Fig. 4. A high-resolution TEM images of DGSL-1 (a) and the SF (enlarged of blue square in (a)) (b)

4. Conclusions

In conclusion, the performance optimization of InGaAs PD with linearly graded $In_xAl_{1-x}As$ buffer layer and DGSLs has been verified in structure by TEM. TDs generated by the lattice mismatch were effectively restrained by the linearly graded $In_xAl_{1-x}As$ buffer layer. Moreover, the DGSLs reduced the conduction band discontinuity in heterojunction interface. The cross-section HRTEM images indicated that the interaction between defects in DGSL layer effectively restrained the motion of the TDs. Finally, the TD density in $In_{0.83}Ga_{0.17}As$ absorption layer was decreased obviously.

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*Corresponding author: zljolly@jlu.edu.cn