# The influence of SiO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> gate insulator to the performance of In-Ga-Zn-O thin film transistors

XINGWEI DING<sup>a</sup>, WEIMIN SHI<sup>a,\*</sup>, JIANHUA ZHANG<sup>b,\*</sup>, HAO ZHANG<sup>b</sup>, JUN LI, XUEYIN JIANG<sup>b</sup>, ZHILIN ZHANG<sup>a,b</sup>

<sup>a</sup>Department of Materials Science, Shanghai University, Shanghai 200072, China

<sup>b</sup>Key Laboratory of Advanced Display and System Application, Ministry of Education, Shanghai University, 200072, China

The authors report on the fabrication of IGZO thin film transistor with SiO<sub>2</sub> or Al<sub>2</sub>O<sub>3</sub> gate insulator. Effects of SiO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> gate insulator for TFT have been investigated. The TFT with SiO<sub>2</sub> gate insulator shows a field effect mobility of 3.6 cm<sup>2</sup>/Vs, a threshold voltage of 4.7 V, an  $I_{on}/I_{off}$  ratio of  $1.6 \times 10^7$ , and a subthreshold swing of 0.46 V/decade; The TFT with Al<sub>2</sub>O<sub>3</sub> gate insulator shows a field effect mobility of 5.2 cm<sup>2</sup>/Vs, a threshold voltage of 3 V, an  $I_{on}/I_{off}$  ratio of  $3.4 \times 10^7$ , and a subthreshold voltage of  $3.4 \times 10^7$ , and a subthreshold swing of 0.37 V/decade respectively. TFTs with low-k insulator have low on-current due to the low-capacitances of the materials. The experiment results show that the type of gate insulators plays an important role in both the field effect mobility and bias stability of the devices. Using high-k insulator is an effective way to decrease the drive voltage for TFT devices.

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# 1. Introduction

Thin-film transistors (TFTs) have received considerable attentions and increasing interests because of their potential application in displays [1, 2]. For the past 10 years thin film transistors (TFTs) made with amorphous and poly silicon have been extensively applied in flat panel display industry [3]. But these TFTs (especially the amorphous silicon ones) actually have some problems: such as light sensitivity and light degradation, low effect mobility and small drain current (typically about 10 µA), which limit their application to other types of flat panel displays such as the organic light emitting diode display (OLED) [4]. Oxide semiconductor thin film transistors (TFT) have recently attracted attention in various electronic device applications [5-7]. Because of their low temperature and low cost process, transparent (wideband gap), and good electric properties (high mobility). Indium gallium zinc oxide (IGZO) have been attracted by many researchers due to their high mobility even thought it has amorphous-phase.

As an important part of a TFT, the gate insulator plays an important role in the TFT performance. TFTs using low-k oxide as the gate insulator have low on-current which is originated from the low capacitance of the low-k oxide [8]. As a conventional low-k dielectric for TFTs, SiO<sub>2</sub> possessing excellent electric stability and leakage current characteristics. However, obtaining low driving voltage TFT based on SiO<sub>2</sub> insulator is still a challenge due to rather low dielectric constant of SiO<sub>2</sub> [9]. Using high-k insulator is an effective way to decrease the drive voltage for TFT devices. It is well known that the output current of a TFT is proportional to the product of the induced carriers (Nc) in the channel and the mobility ( $\mu$ ). The induced carriers (Nc) is determined by the relation of Nc=( $\varepsilon \varepsilon_0/ed$ )/V<sub>GS</sub>, where  $\varepsilon \varepsilon_0$ , d and V<sub>GS</sub> are the dielectric constant, gate insulator thickness and applied gate voltage, respectively. As a result, by using high-k insulator, the large carriers' density can be produced in even at low applied gate voltage, resulting in low drive voltage TFTs [10-16]. Therefore, we have investigated the use of Al<sub>2</sub>O<sub>3</sub> which is one of the most promising high-k materials with high capacitance to improve the TFT performances. Here we report the fabrication of IGZO TFTs with SiO<sub>2</sub> or Al<sub>2</sub>O<sub>3</sub> as the gate insulators to compare their performance.

## 2. Experiments

The TFTs with low-k SiO<sub>2</sub> (named SiO<sub>2</sub>-TFT) and high-k  $Al_2O_3$  (named  $Al_2O_3$ -TFT) gate insulators are fabricated on the n-Si respectively. The TFTs structure used in this study is shown in Fig. 1.



Fig. 1. Schematic structure of the TFTs. (a) SiO<sub>2</sub>-TFT; (b) Al<sub>2</sub>O<sub>3</sub>-TFT.

The  $Al_2O_3$  gate insulator (230 nm) is deposited at 300 <sup>o</sup>C using alternating exposures of Al(CH<sub>3</sub>)<sub>3</sub> and H<sub>2</sub>O vapor at a deposition rate of 0.66 Å per cycle by atomic layer deposition. The SiO<sub>2</sub> gate insulator (260 nm) is deposited by thermally oxide grown. 30 nm thick IGZO film are deposited by rf-magnetron sputtering at room temperature using a IGZO target (99.99%, In<sub>2</sub>O<sub>3</sub>, Ga<sub>2</sub>O<sub>3</sub>, ZnO = 1:1:1 mol%) at input power of 50 W, gas mixing ratio of Ar:O<sub>2</sub> (30/1), and total pressure of 0.8 Pa. After deposition of IGZO layer, about 200 nm Al was deposited by thermal evaporation to form the source and drain electrodes through a shadow-mask with the channel width (W) of 1000 µm and channel length (L) of 50 µm. Thermal annealing was carried out at 300 °C for 40min in atmosphere. The thickness of the film was measured by the alpha step (Dektak 3st). The electrical characteristics of IGZO TFTs with SiO2 or Al2O3 dielectrics were measured using Agilent E3647A Dual output DC power supply and Keithley 6485 Picoammeter and related software. The capacitance characteristics were measured using Agilent E4980A LRC meter.

# 3. Results and discussion

Fig. 2 shows the leakage current characteristics as obtained from 1 mm diameter  $n-Si/SiO_2/Al$  and  $n-Si/Al_2O_3/Al$  dots. Al is used as the top-electrode and n-Si as the bottom-electrode. As is well known, thinner gate insulator may produce serious gate leakage current and low breakdown voltage, which make the  $I_{on}/I_{off}$  ratio poor and the device instable, while much thick gate dielectric will lead to low capacitance and more fixed oxide charges, resulting in lower mobility and higher threshold voltage. From Fig. 2 we can see that the leakage current density of is  $1.8 \times 10^{-6}$  mA/cm<sup>2</sup> and  $2.1 \times 10^{-5}$  mA/cm<sup>2</sup> at 2

MV/cm for n-Si/SiO<sub>2</sub>/Al and n-Si/Al<sub>2</sub>O<sub>3</sub>/Al which indicates that both gate insulator shows good leakage property.



*Fig. 2. The leakage current characteristics.* (*a*) *n-Si/SiO<sub>2</sub>/Al;* (*b*) *n-Si/Al<sub>2</sub>O<sub>3</sub>/Al.* 



Fig. 3. The output characteristics. (a) SiO<sub>2</sub>-TFT; (b) Al<sub>2</sub>O<sub>3</sub>-TFT.

Fig. 3(a) and (b) shows the output characteristics for the TFT with SiO<sub>2</sub> or Al<sub>2</sub>O<sub>3</sub> gate insulator, respectively. All the devices have the n-channel, since the electrons are generated by the positive  $V_{GS}$ . The TFT with Al<sub>2</sub>O<sub>3</sub> shows much lager output ( $I_{DS}$ ) current compared with the SiO<sub>2</sub>-based device. Its saturation current reached 0.43 mA at applied gate voltage ( $V_{GS}$ ) = 20 V and source to drain voltage ( $V_{DS}$ ) =10 V, which is 6.5 times larger than 0.066 mA of SiO<sub>2</sub>-based device. From Fig. 3 (b), we can see that there are some leakage of the Al<sub>2</sub>O<sub>3</sub> based TFT at applied gate voltage ( $V_{GS}$ ) = 0 V due to the bombardment to Al<sub>2</sub>O<sub>3</sub> film from the process of sputtering IGZO film with high power, So adopting a small input power at the beginning of sputtering IGZO will be an effect way to solve this problem.



Fig. 4. Corresponding transfer characteristic  $I_{DS}$  versus  $V_{GS}$  at a fixed  $V_{DS}$  10 V and the  $I_{DS}^{1/2}$ - $V_{GS}$  curves. (a)  $SiO_2$ -TFT; (b)  $Al_2O_3$ -TFT.

Fig. 4 shows the corresponding transfer characteristic  $I_{\rm DS}$  versus  $V_{\rm GS}$  at a fixed  $V_{\rm DS}$  10 V and the  $I_{\rm DS}{}^{1/2}$ - $V_{\rm GS}$  curves of TFT with SiO<sub>2</sub> or Al<sub>2</sub>O<sub>3</sub> gate insulator. The  $I_{\rm on}/I_{\rm off}$  ratio for of SiO<sub>2</sub>-TFT and Al<sub>2</sub>O<sub>3</sub>-TFT are measured to be about 1.6×10<sup>7</sup> and 3.4×10<sup>7</sup>, respectively. From the  $I_{\rm DS}{}^{1/2}$ - $V_{\rm GS}$  curves shown in Fig. 4, the channel mobility ( $\mu_{\rm sat}$ ) and threshold voltage ( $V_{\rm th}$ ) can be extracted according to the expression:

$$I_{DS} = \frac{C_i \mu W}{2L} (V_{GS} - V_{TH})^2 \qquad V_{DS} > V_{GS} - V_{TH} \quad (1)$$

Where  $C_i$  is the capacitance per unit area of the insulator layer ( $C_i \varepsilon$  for SiO<sub>2</sub>-TFT and Al<sub>2</sub>O<sub>3</sub> -TFT are 10 nF/cm<sup>2</sup>;3 and 28.7 nF/cm<sup>2</sup>;7.5 respectively). W and L are the channel width and length,  $V_{DS}$  and  $V_{GS}$  are the drain-source voltage and gate-source voltage, respectively. The field effect mobility and threshold voltage of SiO<sub>2</sub>-TFT and Al<sub>2</sub>O<sub>3</sub>-TFT are estimated to be about 3.6 cm<sup>2</sup>/Vs, 4.7 V and 5.2 cm<sup>2</sup>/Vs, 3 V, respectively. As the result, we confirmed that high-k Al<sub>2</sub>O<sub>3</sub> is useful to operate devices at low gate voltage and this result is useful to the current driving devices.

The sub-threshold voltage swing (SS) can be determined through the relation:

$$SS = \frac{dV_{GS}}{d(LogI_{DS})} \tag{2}$$

Here we get a value of 0.46 V/dec and 0.37 V/dec for  $SiO_2$ -TFT and  $Al_2O_3$ -TFT due to the increase of  $C_i$  results in the reduction of the subthreshold swing [8].

From *SS* we can infer the maximum density of surface states at the channel-insulator interface as:

$$N_{\max}^{SS} = \left[\frac{SLog(e)}{(kT/q)} - 1\right]\frac{C_i}{q} \tag{3}$$

and taking into account the value of  $C_i$ ,  $N^{SS}$ max of  $4.2 \times 10^{11}$  cm<sup>-2</sup> and  $9.3 \times 10^{11}$  cm<sup>-2</sup> are calculated for SiO<sub>2</sub>-TFT and Al<sub>2</sub>O<sub>3</sub>-TFT, respectively. According to the  $N^{SS}$ , we draw a conclusion that the Al<sub>2</sub>O<sub>3</sub>-TFT has lager charge trapping at the channel-insulator interface which leads to more defects than SiO<sub>2</sub>-TFT.



Fig. 5. The transfer curves of TFTs, the gate bias of 10 V was applied for an hour at room temperature in atmosphere (a) SiO<sub>2</sub>-TFT; (b) Al<sub>2</sub>O<sub>3</sub>-TFT.

Fig. 5 shows the transfer curves of TFTs with SiO<sub>2</sub> or  $Al_2O_3$  gate insulator, respectively. The gate bias of 10 V was applied for an hour at room temperature in atmosphere. All the transfer curves show a positive shift by the positive gate voltage stress. The threshold voltage shift is 1 V and 4 V for SiO<sub>2</sub>-TFT and  $Al_2O_3$ -TFT which indicates that IGZO TFT with  $Al_2O_3$  gate insulator is more sensitive to bias stress than IGZO TFT with SiO<sub>2</sub> gate insulator. The reason is that the  $Al_2O_3$ -TFT has more defects than SiO<sub>2</sub>-TFT at the channel-insulator interface.

## 4. Conclusion

In summary, top-contact TFT with SiO<sub>2</sub> or Al<sub>2</sub>O<sub>3</sub> gate insulator were fabricated. And the effects of gate insulator on the performances of IGZO-TFT were investigated. In the SiO<sub>2</sub>-TFT, mobility, threshold voltage, subthreshold swing,  $I_{on}/I_{off}$  ratio, are measured as 3.6 cm<sup>2</sup>/Vs, 4.7 V, 0.46 V/decade,  $1.6 \times 10^7$ , respectively. For Al<sub>2</sub>O<sub>3</sub>-TFT, mobility, threshold voltage, subthreshold swing,  $I_{on}/I_{off}$ , are measured as 5.2 cm<sup>2</sup>/Vs, 3 V, 0.37 V/decade,  $3.4 \times 10^7$ , respectively. After the gate bias of 10 V applied for an hour at room temperature, threshold voltage shift is 1 V and 4 V which turned out that SiO<sub>2</sub>-TFT are very useful to improve the stability of the devices. But, high gate-voltage is necessary to drive the device. Al<sub>2</sub>O<sub>3</sub>-TFT is very useful to reduce the driving voltage of the device. Whereas, they are not stability enough, it is expected that if problems are solved, realization of the device, which is reliable and low power consumption, would be possible.

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#### References

- D. J. Gundlach, Y. Y. Lin, T. N. Jackson, S. F. Nelson, D. Schiom, EEE Electron. Dev. Lett. 18, 87 (1997).
- [2] A. Dodabalapur, L. Torsi, H. E. Katz, Science. 268, 270 (1995).
- [3] Y. Ohya, T. Niwa, T. Ban, Y. Takahashi, Jpn. J. Appl. Phys., Part 1, 40, 297 (2001).
- [4] R. E. I. Schropp, B. Stannowski, J. K. Rath, J. Non-Cryst. Solids. 299, 1304 (2002).
- [5] K. Nomura, H. Ohta, K. Uata, T. Kamiya, M. Hirano, H. Hosono, Science. **300**, 1269 (2003).
- [6] E. Fortunato, P. Barquinha, A. Pimental, A. Goncalves, A. Margues, L. Prerier, R. Martins, Adv. Mater. (Weinheim.Ger.) 17, 590 (2005).
- [7] H. Q. Chiang, J. F. Wager, R. L. Hoffman, J. Jeong, D. A. Kezsler, Appl. Phys. Lett. 86, 013503 (2005).
- [8] Yoon Soo Chun, Seongpil Chang, Sang Yeol Lee, Microelectronic Engineering. 88, 1590 (2011).
- [9] Hoonha Jeon, Kyoungseok Noh, Do-Hyun Kim, J. Korean Phys. Soc. 51 (2007).
- [10] I. D. Kim, Y. W. Choi, H. L. Tuller, Appl. Phys. Lett. 87, 043509 (2005).
- [11] E. Fortunato, P. Barquinha, A. Pinnentel, Thin Solid Films. 487, 205 (2005).
- [12] S. Sasa, M. Ozaki, K. Koike, M. Yano, M. Inoue, Appl. Phys. Lett. 89, 053502 (2006).
- [13] K. Lee, H. K. Jae, I. Seongil, S. Chang, H. Kim, B. Koo, Appl. Phys. Lett. 89, 133507 (2006).
- [14] S. O. Min, D. K. Hwang, K. Lee, I. Seongil, Appl. Phys. Lett. 90, 173511 (2007).
- [15] Dhananjay, S. B. Krupanidhi, J. Appl. Phys. 101, 123717 (2007).
- [16] M. M. De Souza, S. Jejurikar, K. P. Adhi, Appl. Phys. Lett. 92, 093509 (2008).

\*Corresponding author: dingxingwei0532@yahoo.cn dingxingwei@aliyun.com