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The frequency dependent electrical characteristics of Sn/p-InP Schottky barrier diodes (SBDs)

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The frequency and bias voltage dependent of the capacitance-voltage (*C-V*) and conductance-voltage (*G/w-V*) characteristics of Sn/p-InP Schottky barrier diodes (SBDs) were investigated in the frequency range of 100 kHz-7 MHz at room temperature. Experimental data shows that the measured capacitance *(C_m)* and conductance *(G_m/w)* increase with decreasing frequency due to a continuous distribution of (N_{ss}) and the effect of series resistance (R_s). These changes in the C_m and G_m/w especially are found noticeable at low frequencies. The variation of the R_s and N_{ss} for the Sn/p-InP SBD obtained from C_m-V and G_m/ω-V characteristics using Nicollian and Goetzberger and Hill's methods, respectivelly. The distribution profile of R_s-V gives two peaks in the inversion and accumulation region, respectively, at low frequencies and these peaks disappear with increasing frequencies. Also, the energy-density distribution profile of interface states exponentially decreases with increasing frequency. Experimental results confirm that the values of N_{ss} and R_s of the Sn/p-InP SBDs are important parameters which strongly influence the C_m-V and G_m/ω-V measurements.

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1. Introduction

Metal-semiconductor SBDs have a crucial role in the semiconductor devices [1]. In generally, an idealized *C-V* and *G/w-V* characteristics are independent frequency and show an increase in capacitance with increasing bias voltage. In applications, the experimental values of *C* and *G/w* depend on various parameters, such as the insulator layer at metal/semiconductor (M/S) interface, N_{ss}, R_s, barrier formation between metal and semiconductor interface and frequency of ac signal. Especially, both N_{ss} and R_s are important parameters that significantly alter *C-V* and *G/w-V* characteristics from those expected for an ideal Schottky barrier diode [2,3]. Some authors [4-11] have reported an anomalous peak in the forward bias *C-V* characteristics due to the presence of R_s and N_{ss} Since the excess capacitance depends on the frequency, the capacitance peak in *C-V* plot is affected [4,9-13] due to N_{ss}, and their time constant.. In order to determine the values of R_s, there are a lot of suggested methods in literature [2,14-16]. Among them the most important one is the conductance technique, developed by Nicollian and Goetzberger [2]. In this technique, frequency dependent of the forward and reverse-bias *C-V* and *G/w-V* measurements give the important information about the distribution interface states and series resistance of SBDs. Therefore, in this study, to determine accurate values of R_s and N_{ss}, we have applied the methods developed by Nicollian and Goetzberger [2] and Hill-Coleman [17], respectively.

In this study, the frequency dependence of *C-V* and *G/ω-V* characteristics of SBDs have been investigated by considering both the N_{ss} and R_s effects in the wide frequency range of 100 kHz-7 MHz (from -5 to 2 V) at room temperature. Experimental results show that both the R_s and N_{ss} are important parameters, which changes the electrical characteristics of of Sn/p-InP Schottky barrier diodes (SBDs).

2. Experimental procedure

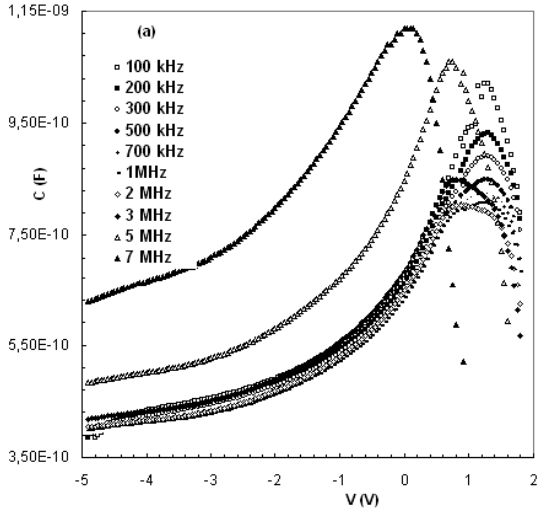
The Sn/p-InP Schottky barrier diodes (SBDs) were fabricated on 2 inch diameter float zone (100) p-type (Zn doped) single crystal InP having thickness of 350 μm with 4-8x10^{17} cm^{-3} carrier concentration given by the manufacturer. Before making ohmic and rectifier contacts, the p-InP wafer was dipped in 5 H_2SO_4+H_20_2+ H_20 solution for 1.0 min to remove surface damage layer and undesirable impurities and then in H_20+HCl solution and then followed by a rinse in de-ionized water with a resistivity of 18 MΩ cm. In order to prevent undesirable any oxidation the wafer was dried with high-purity nitrogen and inserted into the deposition chamber immediately after etching process. The back side of the

p-type InP was formed by sequentially evaporating Zn and Au layers on InP in a vacuum-coating unit of 10^{-6} Torr. After that, low resistance ohmic contact InP wafer was formed by sintering the evaporated Zn and Au layers at 350 ºC for 3 min in flowing N_2 in a quartz tube furnace. Finally, the Schottky contacts were formed by evaporating Sn dots with diameter of about 1mm on the front surface of the p-InP.

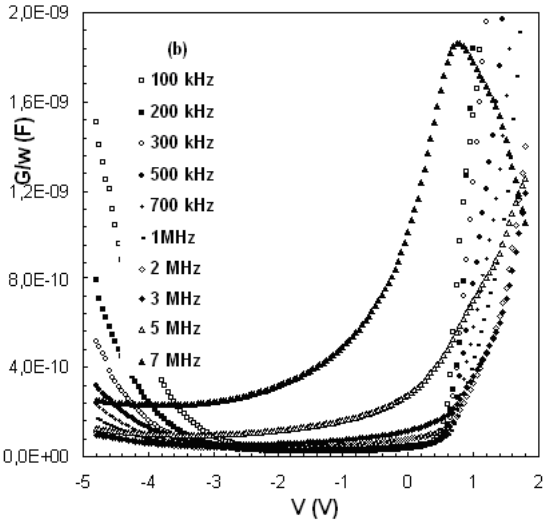
After fabricated process of the Sn/p-InP Schottky barrier diodes (SBDs), their frequency dependent *C-V* and conductance-voltage *G/ω-V* measurement are carried out in the frequency range of 100 kHz-7 MHz by using HP 4192A LF impedance analyzer and a small sinusoidal signal of 40 mV_{p-p} from the external pulse generator is applied to the sample in order to meet the requirement [2]. All experimental measurements were controlled by help of a microcomputer through an IEEE-488 ac/dc converter card in the dark.

3. Results and discussion

In order to clarify the effect of series resistance and interface states on high frequency capacitance-voltage (*C-V*) and (*G/w-V*) characteristics of Sn/p-InP Schottky barrier diode, these measurements were carried out at the frequency range of 100 kHz-7 MHz at room temperature and were given in Fig. 1 (a) and (b), respectively. The applied bias voltage was swept from -5 V to 2 V with 50 mV steps. As shown in Fig. 1 (a) and (b) the measured capacitance and conductance are strongly dependent on bias voltage and frequency. Both the high values of *C* and *G/w* in the forward bias region at low frequencies may be attributed to the series resistance (R_s) and excess capacitance (C_{ex}) resulting from the surface states (N_{ss}) in equilibrium with InP and their relaxation time. Therefore, the *C-V* curves (Fig. 1 (a)) vary from the inversion region to accumulation region in the frequency range of 100 kHz-7 MHz at room temperature and give an anomalous peak in the forward bias/accumulation region in each frequency due to the existence of series resistance. Similarly, Fig. 1(b) shows the variation of the measured conductance (G_m/w-*V*) in the depletion region for the same frequency interval, indicating the existence of different carrier life time (τ) dependent responses of interface states. At high frequencies (the carrier life time τ is much larger than the period of frequency$1/2\pi f$) the charge at interface states cannot follow an ac signal contrary to low frequencies [2,3]. Such behavior of *C* and *G/w* indicate the presence of continuous distribution of the interface states, resulting in a progressive decrease of response of the interface state to applied ac voltage [2-4,8].



(a)



(b)

Fig.1 The frequency dependent plots of (a) the capacitance-voltage and (b) conductance-voltage characteristics of Sn/p-InP SBD at room temperature.

Series resistance (R_s) causes a serious error in the extraction of interfacial properties from the *C-V* and *G/w-V* characteristics of the semiconductor devices such as metal-semiconductor (MS) and metal-insulator-semiconductor (MIS) or (MOS) structures. This error can be minimized by measuring the series resistance and applying a correction to the measured capacitance (C_m) and conductance (G_m/w) values before the desired information is extracted [2-5]. In order to extract the real series resistance (R_s) of these devices, several methods have been suggested in literature [2,14-16]. In this study, for our Sn/p-InP Schottky barrier diode, we have applied

the admittance technique [2]. According to this method, the real series resistance of these structures can be subtracted from the measured capacitance (C_m) and conductance (G_m/w) in strong accumulation region at high frequencies (f ≥1 MHz) [3].

$$R_s = \frac{G_m}{G_m^2 + \left(\omega\ C_m\right)^2} \qquad (1)$$

Also, voltage dependence of the series resistance (R_s) can be obtained from the measurements of *C-V* and *G/ω-V* curves at various applied bias and frequencies as

$$R_s(V) = \frac{G_m(V)}{G_m^2(V) + \left(\omega\ C_m(V)\right)^2} \qquad (2)$$

where C_m and G_m represent the measured capacitance and conductance at given any applied bias voltage. In generally, the major error in the C_m and G_m occurs in the accumulation region due to series resistance and a portion of the depletion region due to interface states.

Therefore, the voltage dependent series resistance is calculated according to Eq. (2) and shown in Fig. 2 for various frequencies. It can be clearly seen from the Fig. 2, the series resistance gives two peaks especially at low frequencies which are located in the inversion and accumulation regions, respectively. While the first peak shifting toward positive bias region, the second peak shifting toward negative bias region. The magnitudes of these peaks increase with decreasing frequency. Such behavior of the R_s is attributed to the particular distribution density of interface states located at metal/insulator interface and insulator layer at metal/semiconductor interface. This frequency dependency of series resistance profile versus voltage is similar to the temperature dependence of series resistance profile versus voltage [4,18-20]. These behaviors show that the carriers have enough energy and time constant to escape from the traps located at semiconductor/insulator interface in the InP band gap. In other word, at low frequencies, the charges at the interface states can easily follow the ac signal contrary to high frequencies [1-4]. As can be seen in Fig. 2, the values of R_s are independent of bias voltage at sufficiently high frequencies. Such behavior of R_s is a result of N_{ss} cannot follow the ac signal and consequently cannot contribute of Sn/p-InP SBD capacitance and conductance.

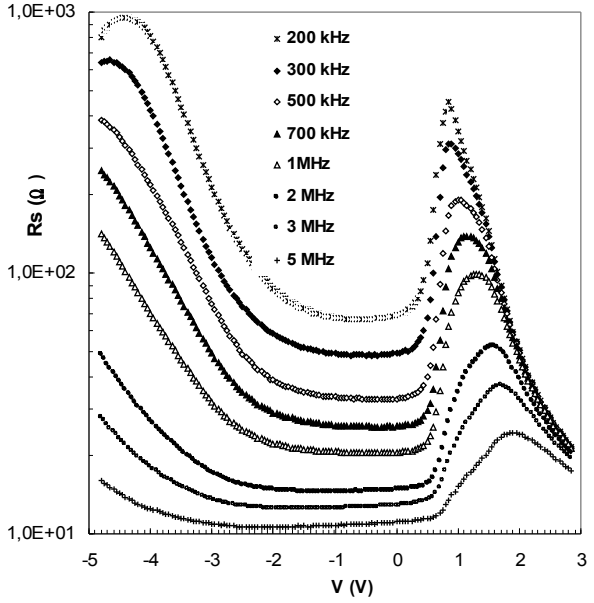


Fig.2 The variation of the series resistance of Sn/p-InP SBD as a function of voltage for various frequencies at room temperature.

According to the Hill-Coleman [17], the density of interface states can be obtained from as

$$N_{ss} = \left(\frac{2}{qA}\right)\frac{(G_m/\omega)_{\max}}{(G_m/\omega)_{\max} C_{ox})^2 + (1 - C_{\max}/C_{ox})^2} \qquad (3)$$

where, A is diode area, ω is the angular frequency ($2\pi f$), C_{max} and $(G_m/\omega)_{\max}$ are the measured C and G/ω which correspond to peak values, respectively, and C_{ox} is the capacitance of insulator layer. The values of R_s and N_{ss} for the Sn/p-InP SBD determined from *C-V* and *G/ω-V* measurements in the frequency range of 100 kHz-7 MHz are given in Table 1. As shown in Table 1, the peak value of capacitance (C_m) and conductance (G_m/w) are found decrease with an decreasing series resistance (R_s) value except for high frequencies (f≥2 MHz). The peak position of C_m shifts toward negative bias region. Similar results are reported in the literature [9,11].

The frequency dependent of interface states density and series resistance profile of the Sn/p-InP SBD are given in Table 1 and Fig. 3. It can be seen in Fig. 3 and Table 1,

both the R_s and N_{ss} values are strongly depend on frequencies and changes become important at low frequencies.

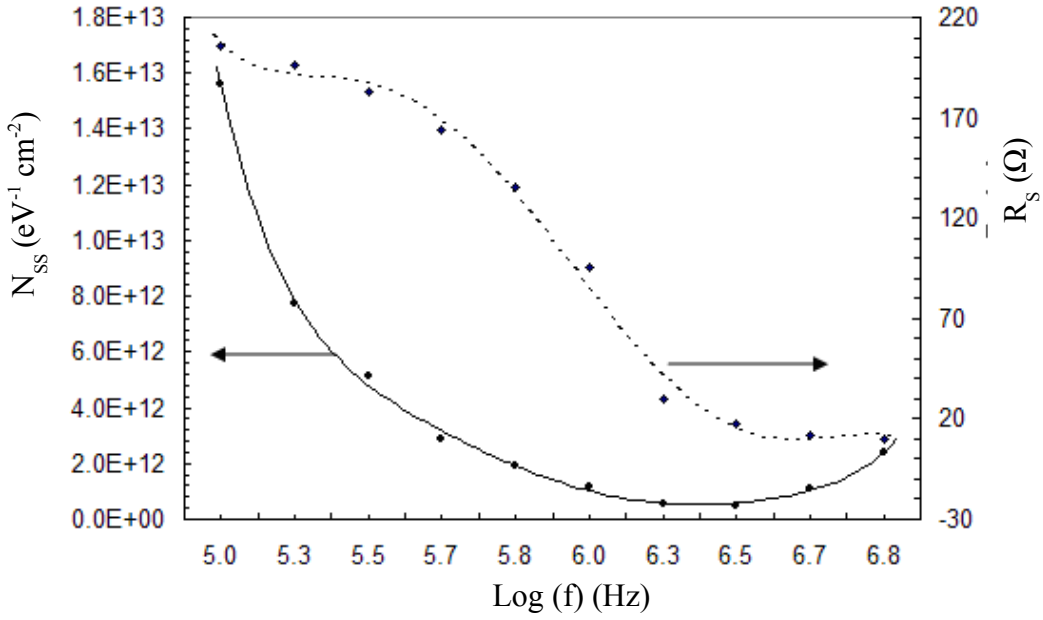


Fig. 3 The variation of the interface states density (N_{ss}) and series resistance (R_s) for the Sn/p-InP SBD obtained from C_m-V and G_m/ω-V characteristics in the frequency range of 100 kHz-7 MHz at room temperature.

Table 1. The values of various parameters for the Sn/p-InP SBD obtained from C-V and G/ω-V characteristics in the frequency range of 100 kHz-7 MHz at room temperature.

f (kHz)	V_m (V)	C_m (nF)	G_m/ω (nF)	N_{ss} ($eV^{-1}cm^{-2}$)	R_s (Ω)
100	1.35	1.02	7.59	$1.56x10^{13}$	206.07
200	1.35	0.93	3.84	$7.71x10^{12}$	195.80
300	1.30	0.89	2.59	$5.15x10^{12}$	183.29
500	1.25	0.84	1.45	$2.85x10^{12}$	163.86
700	1.20	0.82	0.98	$1.91x10^{12}$	135.71
1000	1.15	0.80	0.61	$1.19x10^{12}$	95.04
2000	0.90	0.80	0.26	$5.21x10^{11}$	29.71
3000	0.80	0.85	0.25	$5.07x10^{11}$	17.36
5000	0.70	1.06	0.52	$1.08x10^{12}$	11.88
7000	0.15	1.12	1.12	$2.37x10^{12}$	10.16

These behaviors were attributed to the excess capacitance resulting from the N_{ss}, which is in equilibrium with the semiconductor that can easily follow the ac signal.

4. Conclusions

In order to good interpret the effects of the interface state density (N_{ss}) and series resistance (R_s) on *C-V* and *G/ω-V* characteristics of the Sn/p-InP SBDs, these measurements are carried out in the frequency range of 100 kHz-7 MHz. Experimental results show that both measured *C* and *G/w* quite sensitive to frequency due to a continuous distribution of N_{ss} and R_s. Such behavior of C_m and G_m/w can be attributed to interface states can easily follow the ac signal, at low frequencies and yield an excess capacitance and conductance, which depend on the relaxation time of the Nss. The variation of the R_s and N_{ss} for the Sn/p-InP SBD were obtained from measurements of *C and G/ω* values in the frequency range of 100 kHz-7 MHz at room temperature using Nicollian and Goetzberger and Hill's methods, respectively. The values

of R_s and N_{ss} exponentially decrease with increasing frequency. In conclusion, we can say that both the values of R_s and N_{ss} are important parameters which strongly affect the *C-V* and *G/w-V* characteristics of the Sn/p-InP SBD.

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