The effects of eutectic force to interconnect characteristics and thermal performances of HP-LED

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Heat dissipation is regarded as the key issue for high power light emitting diode (HP-LED) packaging. Silver paste can hardly dissipate the heat effectively for its low thermal conductivity coefficient. Though the eutectic processes are complicated, eutectic interconnect is an effective way to improve the heat dissipation. The effects of eutectic force to interconnect characteristics and thermal performances of HP-LED are investigated in this paper. The optical and thermal performances of the HP-LED interconnected with different eutectic force are tested and analyzed. The results show that the eutectic force is indeed needed to improve the thermal and optical performances.

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Keywords: HP-LED, Eutectic interconnect, Eutectic force, Junction temperature

1. Introduction

Silver paste is the conventional interconnect material for HP-LED chip packaging. But it is hardly to dissipate the heat efficiently, because the heat dissipation of the HP-LED becomes more and more challengeable with the increasing requirement for high electrical power input. The thermal conductivity of metal eutectic interconnect material can be as high as 60 W/mK. So there are more and more attentions focus on the investigations of metal eutectic interconnects. Better interconnected performances have been proved, such as lower thermal resistance compared to devices interconnected by solder paste and silver paste [1,2]. The gold tin eutectic interconnect technology is well developed in the field of miro-electronics, such as the thin Si wafers and Cu laminated polyimide films bonding [3], high power laser diode bonding boron nitride heat sinks [4], silicon-to-alumina bonding [5] and so on [6-9]. Matijasevic has investigated the Void free bonding between GaAs dice and alumina substrates. The results show that there are no cracks on the GaAs dice after thermal shock and thermal cycle test [10]. The reliability mechanism investigation of eutectic interconnect of SnAgCu is investigated by Chun and Wiese [11-13]. As the HP-LED chip is different to microelectronics, HP-LED eutectic interconnect processes are complicated and void in the interconnect layer is tend to generate. The void ratio will cause the increase of junction temperature which will affect the reliability. Fleischer and Ciampolini have investigated the effects of void ratio to the thermal resistance [14,15]. The results show that the thermal resistance can be effectively affected by the void ratio. Park has investigated the Au20Sn solder joint between a HB-LED and a Si heat sink by transmission electron microscopy (TEM) analysis. The research results showed that limited amount of solder and low bonding force, inadequate solder wetting can cause numbers of void in the solder and at the interface [16]. Processing parameters for die attach process of Au20wt%Sn eutectic solder metallization has been studied. The key factors of the process are die metallization structure design, bonding/reflow temperature and substrate pad metallization [17]. The top surface of the HP-LED chip is a lighting surface, though gold tin eutectic bonding has been proved to be with lower thermal resistance [18], but there are still some challenges for HP-LED eutectic interconnect. In order to investigate the effects of eutectic force to the HP-LED thermal performances, an improved eutectic process with different eutectic force is designed for the eutectic interconnects. The eutectic model is as Fig. 1, it is bottom heated and upper surface forced during the eutectic interconnects.

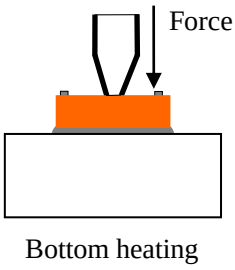


Fig. 1. LED eutectic process with force.

2. Experiments

In order to simplify the HP-LED structure, the substrate is designed and fabricated with ceramic substrate, the circuit layer is copper layer with gold coating layer, such as Fig. 2.

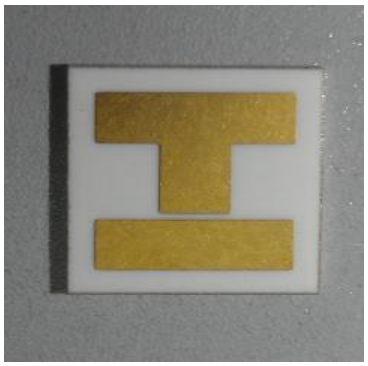


Fig. 2. The designed substrate.

In the experiments, the HP-LED chip is EZ-900 series from CREE. The structure of the chip and the substrate is as Fig. 3.

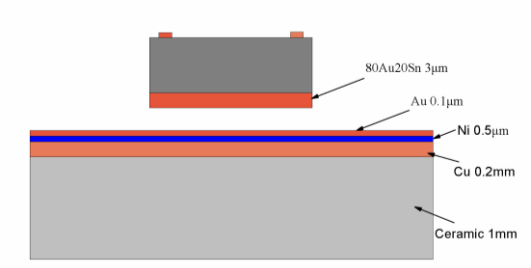


Fig. 3. Parameters of the substrate and LED chip for eutectic interconnect process.

In order to investigate the effects of eutectic force to the void ratio of HP-LED, four eutectic force parameters are selected. The four parameters are 0 N, 0.15 N, 0.3 N, 0.45 N. Five HP-LED samples are packaged for each eutectic force process. The packaged HP-LED is as Fig. 4.

Fig. 4. LED devices interconnected by 80Au20Sn.

The thermal performances and optical performances are both tested for the HP-LEDs with different eutectic parameters.

3. Results and discussion

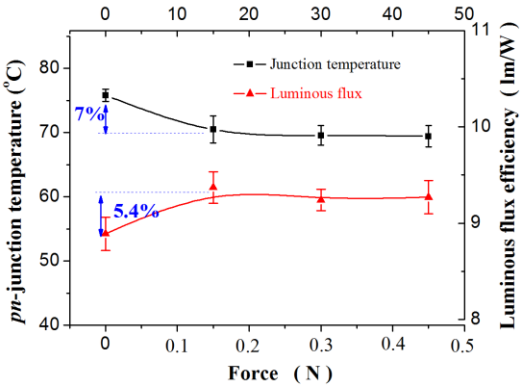


Fig. 5. Effects of eutectic force on the pn junction temperature and luminous flux of HP-LED.

Fig. 5 illustrates the effects of eutectic force on the *pn*-junction temperature and luminous flux of the HP-LEDs interconnected by different eutectic force. From Fig. 5, the *pn*-junction temperature decreases from 75 °C to 70.5 °C and the luminous flux efficiency increased from 8.89 lm/W to 9.37 lm/W with the eutectic force increases from 0 N to 0.15 N. The *pn*-junction temperature and luminous flux efficiency be improved about 7% and 5.4%, respectively. But the *pn*-junction temperature and the luminous flux efficiency improvements are not clearly with the eutectic force increases from 0.15 N to 0.45 N. For luminous flux efficiency, 5.4% improvement is for blue light. As the YAG phosphor emission intensity is greatly dependent on the working temperature, it will decrease with the temperature increase. This is attributed to the increase of the non-radiative relaxation rate which can be explained by the luminescent material decay time formula [19]:

$$\tau = (\gamma_r + \gamma_{nr})^{-1} \quad (1)$$

Where γ_r and γ_{nr} are radiative relaxation rate and non-relaxation rate respectively.

The γ_{nr} increases with the increase of the working temperature. For the HP-LED with eutectic force in the experiments, the 7% improved *pn*-junction temperature will also improve the phosphor emission intensity which will benefit the white light emission efficiency.

In order to investigate the effects of the eutectic force to the interconnect layer thickness, HP-LEDs interconnected with different eutectic force are cut along the vertical direction of the HP-LED chip. Then the cutting surfaces are polished preparing for the thickness measurement by optical microscope (LEICA DM2500M) and scanning electron microscope (SEM) test.

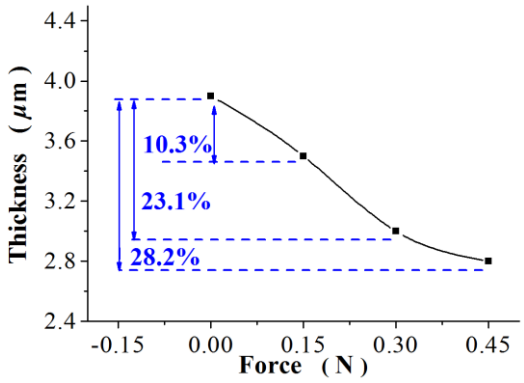


Fig. 6. Relationship between the thickness of the interconnect layer and the eutectic force.

Fig. 6 shows the relationship between the thickness of interconnect layer and the eutectic force. With the increase of the eutectic force, the thickness shows a decrease trend. By the reference of this relationship, the thickness with eutectic force of 0.45 N is good for the thermal resistance. But for particular samples, there are cracks on the HP-LED chip surface with eutectic force of 0.45 N. The cracks on the HP-LED chip top surface are as Fig. 7.

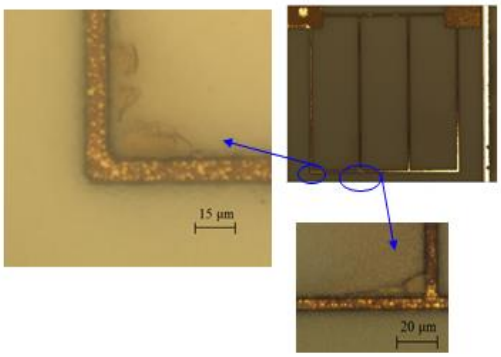
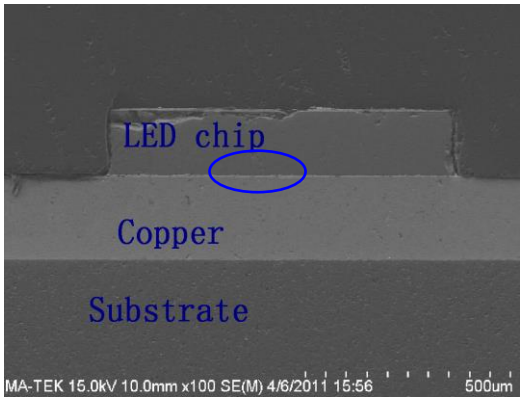
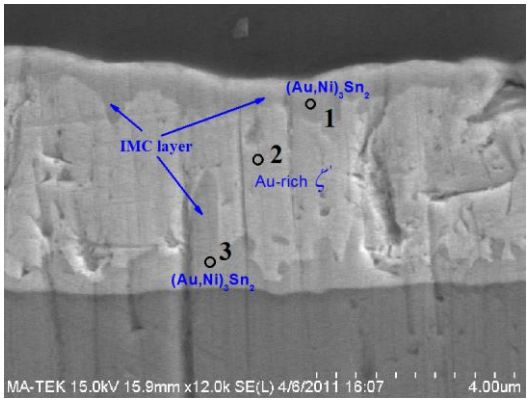


Fig. 7. Cracks on LED chip surface with eutectic force of 0.45 N.

At last, SEM is used to analyze the interconnect characteristics of the eutectic interconnect layer HP-LED. The cross-section structure and eutectic interconnect layer of HP-LED with 0.15 N force is as Fig. 8.



(a)

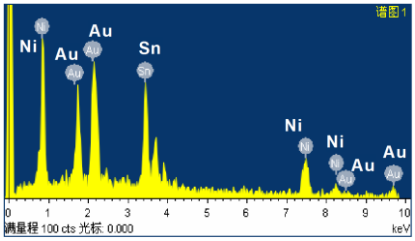
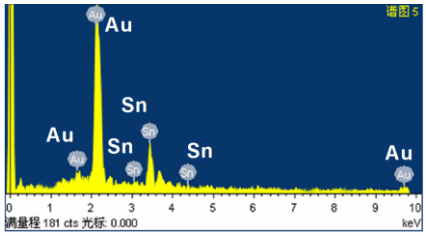
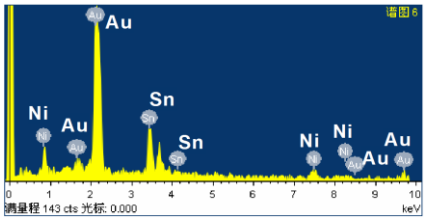


(b)

Fig. 8. Eutectic interconnect layer of LED with 0.15 N force: (a) Cross section of LED eutectic layer (b) Enlarged drawing of eutectic interconnect layer.

Three points in the eutectic layer (number 1, number 2 and number 3) are tested by Energy Dispersive X-ray Spectrum (EDX). The tested results are listed in Table 1.

Table 1. EDX tested results of eutectic interconnect layer of LED with 0.15 N force.

Points number	Energy dispersive spectrum	Element proportion
1		element / wt.% / at.% Ni K 26.36 47.40 Sn L 37.13 33.03 Au M 36.51 19.57 sum 100.00 ~$(Au,Ni)_3Sn_2$+Ni
2		element / wt.% / at.% Sn L 24.045 34.44 Au M 75.95 65.56 Sum 100.00
3		element / wt.% / at.% Ni K 8.04 19.64 Sn L 27.91 33.72 Au M 64.05 46.64 sum 100.00 ~$(Au,Ni)_3Sn_2$+Ni

By Table 1, it is clearly that the intermetallic compound (IMC) (Au,Ni)3Sn2 is formed. The IMC layer is with light gray color which distributed along the eutectic layer edge, such as point 1 and point 3. It is mainly located at the interface between the HP-LED chip bottom surface and the interconnect layer, the interface between substrate top surface and the interconnect layer. In the middle of the eutectic interconnect layer, the gray-white color structure is mainly the Au-rich phase, such as point 2. As the Au-rich phase is with good mechanical strength, the SEM results showed that the eutectic interconnect layer is successfully formed.

4. Conclusions

With eutectic force increases from 0 N to 0.15 N, the junction temperature and optical performances can be improved 7% and 5.4% respectively. With eutectic force keeping increase to 0.45 N, the interconnect thickness can be decreased, but the improvements of junction temperature and optical performances are not obvious and cracks are found on the surface of particular HP-LED chip samples. The results show that the eutectic force is indeed needed to improve the junction temperature, but not too much. By the image of SEM test, the IMC (Au,Ni)3Sn2 is formed at the interface between the bottom of HP-LED chip and the interconnect layer and the interface between top substrate surface and the interconnect layer.

Acknowledgments

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