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The effect of series resistance and surface states on current-voltage (*I-V)* characteristics of Au/n-GaAs/GaAs structures at wide temperature range

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The forward and reverse bias current-voltage (*I-V)* characteristics of Au/n-GaAs/GaAs have been measured in the temperature range of 79-400 K. The effects of density of interface states N_{ss} and the series resistance R_s of structures on the electrical characteristics are investigated as a function of temperature. While the zero-bias barrier Φ_{Bo} decrease, the ideality factor n increases with a decrease in temperature; the changes are quite significant at low temperatures. Experimental results show that the R_s and N_{ss} cause non-ideal behavior on *I-V* characteristics. The R_s is significant especially in the downward curvature of the forward bias *I-V* characteristics, but the N_{ss} are significant in both the linear and non-linear regions of the *I-V* characteristics. The downward concave curvature of the forward bias *I-V* curves at sufficiently high voltages has been attributed to the presence of R_s, apart from the N_{ss} that are in equilibrium with the semiconductor. The high value of the ideality factor n and the Schottky barrier height Φ_{Bo} of these structures were attributed to the presence of an interfacial insulator layer between metal and semiconductor. The density of interface states distribution profiles (N_{ss}) as a function of (E_c-E_{ss}) was obtained from the forward bias *I-V* measurements by taking into account the bias dependence of the effective barrier height Φ_e and ideality factor n at different temperatures for the sample on the order ~10^{13} $eV^{-1}cm^{-2}$. In addition, the values of n, Φ_{Bo} and R_s of these structures have been obtained at each temperatures using Cheung's functions.

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1. Introduction

In generally, the forward bias current-voltage (*I-V*) characteristics of metal-semiconductor (MS) or metal-insulator-semiconductor (MIS) contacts are linear on a semi-logarithmic scale at intermediate forward bias voltage but deviate considerably from linearity due to the effect of series resistance R_s and the density of interface states N_{ss} when the applied voltage is sufficiently high. The temperature dependence of main diode parameters such as barrier height Φ_{Bo}, ideality factor n, series resistance R_s and density of interface states N_{ss} are obtained from the forward bias *I-V* characteristics show abnormal behavior, for example, the Φ_{Bo} obtained from *I-V* measurements using standard thermionic emission (TE) theory decreases and the n increases with decreasing temperature. Thus, the standard TE theory fails to explain such behavior. Especially, the changes are more significant at low temperatures. Because, at low temperatures the lower barrier patches carry a large fraction of the current. The performance and reliability of MS and MIS type devices especially depend on the formation of insulator layer between metal and semiconductor interface, the density of interface states N_{ss}, series resistance R_s and an inhomogeneous barrier height. The R_s is significant especially in the downward curvature of the forward bias *I-V* characteristics, but the N_{ss} is significant in both the linear and non-linear regions of the *I-V* characteristics. When a forward bias V is applied across the diode, the value of V will be shared by the R_s, interfacial insulator layer and depletion layer. Both the lower R_s and N_{ss} the greater the range over which the *I-V* yields at a straight line [1,2].

In general, surface states divide into two groups and one of these groups communicates most rapidly with the metal, the other group with the semiconductor [3]. This is a result of distribution of the N_{ss} in space as well as in energy over the GaAs forbidden band gap of the semiconductor. The N_{ss} in each of these groups are dependent upon the natural thickness of the insulator layer (between metal and semiconductor) and communication with semiconductor increases with increasing insulator layer thickness. Also the increase in the value of ideality factor n due to interfacial insulator layer is well know and can be understood in terms of surface states which do not equilibrate with the metal and the potential drop across the insulator layer [3]. Due to the technological importance of such devices, there are a great number of studies have been made in last few decades [4-28]. The popularity of these studies, which is rooted in their importance to the semiconductor industry, does not assure uniformity of the results or of interpretation.

Horvarth [4], independently from Card and Rhoderick [3], derived an expression for the ideality factor n, giving the contribution of the interfacial insulator layer and surface states to Schottky barriers lowering but forward

and reverse bias and evaluated the interface state energy distribution and the relative interfacial insulator layer thickness. In addition, the characterization of R_s and N_{ss} in MS or MIS type Schottky diodes have become a subject of very intensive research and reported in the literature for more than four decades [2,3,5-7].

In the previous work we have reported the predominant carrier transport mechanisms in MBE grown epitaxial Au/n-GaAs/GaAs structures [8], and in this work we report the results of systematic investigation on the temperature dependence of the electrical properties of MBE grown epitaxial Au/n-GaAs/GaAs structures. The forward bias and reverse bias *I-V* measurements of these structures were carried out over the temperature range 79-400 K. The density of interface states distribution profiles (N_{ss}) as a function of (E_c-E_{ss}) was obtained from the forward bias *I-V* measurements by taking into account the bias dependence of the effective barrier height Φ_e and ideality factor at different temperatures. Also the values of the series resistance R_s were extracted from the forward bias I-V curves using Cheung's method.

2. Experimental procedure

The n-GaAs/GaAs structure was grown by VG80H solid source molecular beam epitaxy (MBE) system. In MBE system, firstly 5000 Å undoped GaAs buffer layer was grown on Zn-doped (100) GaAs substrate. Then, Si-doped n-type 5000 Å $Al_{0.24}Ga_{0.76}As$ and n-type Si doped GaAs epilayers was grown. The sample was dipped in methanol and deionized water sequentially for 10 min each for the removal of organic impurities from the surface of the sample. Then, it was dipped in H_2SO_4+H_2O_2+H_2O (1:1:300) for 5s to remove the native oxide layer from the back surface and then followed by a rinse in the deionized water resistivity of 18 MΩcm. After the etching process, the wafer was dried with high purity dry nitrogen (N_2) and immediately inserted into the vacuum chamber. Immediately after surface cleaning, high purity gold (Au) metal (99.999%) with a thickness of 2000 Å was thermally evaporated from the tungsten filament onto the whole back surface of the wafer in the pressure of ~10^{-6} Torr. The ohmic contact was formed by sintering the evaporated Au back contact at 400 ^{o}C for 90 min in a flowing dry nitrogen ambient at a rate of ~2 l/min. In addition, the contact was tested whether or not performs ohmic contact using current-voltage (I-V) measurements. As a result, upon heating 400 ^{o}C, 90 min the contact become truly ohmic. Immediately after ohmic contact, circular dots shaped Au Schottky (rectifier) contacts with area about 0.011 cm^2 and 2500 Å thickness were formed by evaporating of Au in the pressure of ~10^{-6} Torr. In this way, few SBDs of the Au/n-GaAs/GaAs structures were fabricated [28]. The native interfacial insulator thickness δ was estimated to be about δ=47 Å from measurement of the insulator capacitance in the strong accumulation region. The forward bias current-voltage (I-V) characteristics of Au/n-GaAs/GaAs SBDs at various temperatures were measured in the temperature range of 79-400 K using temperature controlled Janes 475 cryostat. I-V measurements of the prepared samples were performed using a Keithley 220 programmable constant current source and a Keithley 614 electrometer. The sample temperature was always monitored by using a copper-constantan thermocouple and a lakeshore 321 auto-tuning temperature controller with sensitivity better than ± 0.1 K. All measurements were carried out with the help of a microcomputer through an IEEE-488 ac/dc converter card.

3. Results and discussion

When a forward bias V is applied across the metal-semiconductor junction, V will be shared by the diode and series resistance. In this case, Thermionic Emission (TE) model for the relationship between forward bias voltage and current of a Schottky diode can be written as follows [5,12,13].

$$I = I_o exp\left(\frac{q}{nkT}(V - IR_S)\right)\left[1 - exp\left(-\frac{q}{kT}(V - IR_S)\right)\right] \quad (1)$$

where I_o is the reverse saturation current and described by

$$I_o = AA^{*}T^{2} exp\left(-\frac{q\Phi_{Bo}}{kT}\right) \quad (2)$$

where the quantities IR_s, A, A^*, T, q, k and Φ_{Bo} are the terms is the voltage drop across series resistance of diode, the rectifier contact area, the effective Richardson constant (8 A/cm^{2}K^2 for n-type GaAs), temperature in Kelvin, the electronic charge, Boltzman's constant and the apparent barrier height at zero bias, respectively. The semi-logarithmic forward and reverse bias *I-V* characteristics of one of the Au/n-GaAs/GaAs structures at various temperatures, ranging from 79 to 400 K are shown in Fig. 1.

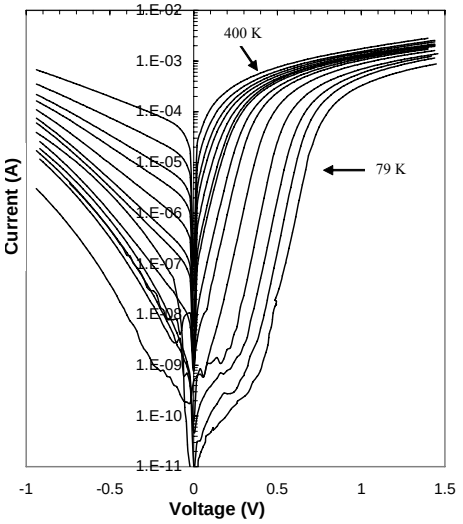

Fig. 1. Experimental forward and reverse bias semi-logarithmic I-V plots of the Au/n-GaAs/GaAs structure in the temperature range of 79-400 K.

The saturation current I_o was obtained by extrapolating the linear intermediate voltage region of the part of linear curve to zero applied voltage and the Φ_{Bo} values were calculated from Eq. (2) and were shown in Table 1. The ideality factor values were obtained from forward bias *ln(I)-V* characteristics through the relation shown in Table 1.

$$n = \frac{q}{kT}\frac{dV}{dln(I)} \tag{3}$$

Also voltage dependent ideality factor *n(V)* can be derivate from Eq. (1) as

$$n(V) = \frac{qV}{kTln(I/I_o)} \tag{4}$$

Our sample with large value of *n* is far from ideal (*n*=1) due to the presence of a thick interfacial oxide layer and the interface states. As shown in Table 1 and in Fig. 2 the experimental Φ_{Bo} values of the Au/n-GaAs/GaAs structure calculated from *I-V* characteristics shows an unusual behavior that it increases with the increase of temperature.

Table 1. Temperature dependent value of various parameters obtained from forward bias I-V characteristics of Au/n-GaAs/GaAs structure in the temperature range of 79-400 K.

T (K)	I_o (A)	n (I-V)	Φ_{Bo}(I-V) (eV)	Φ_B(T) (eV)
79	4.00×10^{-15}	3.97	0.292	1.159
110	1.55×10^{-14}	2.91	0.403	1.170
140	6.55×10^{-14}	2.42	0.504	1.180
170	1.37×10^{-12}	2.02	0.576	1.100
200	8.52×10^{-11}	1.81	0.615	0.960
230	9.10×10^{-10}	1.52	0.669	0.888
260	7.85×10^{-9}	1.41	0.716	0.876
290	5.84×10^{-8}	1.30	0.757	0.880
300	1.04×10^{-7}	1.27	0.771	0.848
320	3.28×10^{-7}	1.20	0.796	0.852
340	1.03×10^{-6}	1.19	0.817	0.854
360	2.14×10^{-6}	1.14	0.848	0.790
380	5.44×10^{-6}	1.10	0.870	0.744
400	1.21×10^{-5}	1.01	0.893	0.740

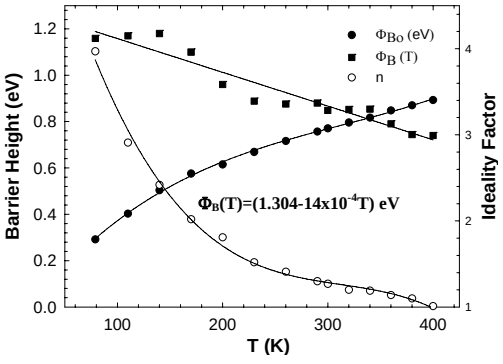

Fig. 2. The zero-bias barrier height $\Phi_{Bo,}$ corrected barrier height $\Phi_B(T)=n\Phi_{Bo}$ and the ideality factor n obtained from forward bias I-V data as a function of the temperature.

While the zero-bias barrier height Φ_{Bo} increases, the ideality factor *n* decreases with increase in temperature; the changes are quite significant especially at low temperatures. The values of zero bias barrier height increases with increasing temperature (Fig. 2). Such temperature dependence is an obvious disagreement with the reported the negative temperature coefficient of the barrier height or forbidden band gap of GaAs. As a result, because of these behaviors saturation current expression in the Eq. (2) must include the ideality factor. The experimental $\Phi_{Bo}(I\text{-}V)$ values multiply with ideality factor *n* to obtain corrected barrier height $\Phi_B(T)=n\Phi_{Bo}(I\text{-}V)$. The $\Phi_B(T)$ values are given in Table 1 and Fig. 2. As can be seen from Table 1, the corrected values of the barrier height $\Phi_B(T)$ decreases with increasing temperature (Fig. 2) and the temperature coefficient values of -14×10^{-4} eV/K is close agreement with the temperature coefficient of the barrier height [12,16,29].

The non-linearity of *I-V* characteristics at high bias values indicates a continuum of interface states in equilibrium with semiconductor [3]. The effective barrier height Φ_e is given as:

$$\Phi_e = \Phi_{Bo} + \beta(V - IR_S) = \Phi_{Bo} + \left(1 - \frac{1}{n(V)}\right)(V - IR_S) \tag{5}$$

by considering the applied voltage dependence of the barrier height. Where β is the voltage coefficient of the effective barrier height Φ_e used in place of the barrier height Φ_{Bo} and it is a parameter that combines the effects of both interface states in equilibrium with the semiconductor. For metal-semiconductor (MS) Schottky diode with an interfacial insulator layer and interface states the ideality factor *n* becomes greater than unity (n=1), as proposed by Card and Rhoderick [3], and is given by

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_S}{W_D} + qN_{SS}\right] \tag{6}$$

Thus, the values of interface states density N_{ss} in equilibrium with semiconductor were obtained by substituting the voltage dependent *n* values. $\varepsilon_s=12.4\varepsilon_o$, $\varepsilon_i=3.5\varepsilon_o$, $\delta=47$ Å and W_D, the width of the space charge region in Eq. (6) at each temperature and is given in Fig. 3 and this expression is identical to Eq. (18) of Card and Rhoderick [3] and Eq.(10) of Çetinkara et al. [14].

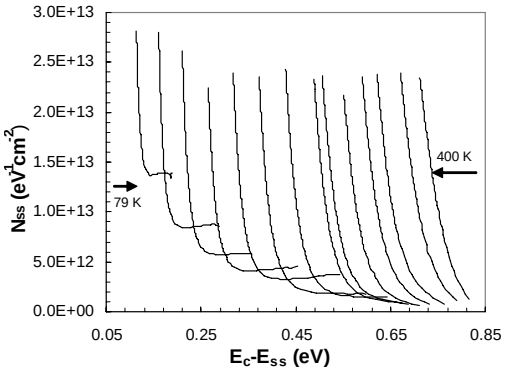

Fig. 3. The density of interface states N_{ss} as a function of E_c-E_{ss} obtained from the forward bias I-V data at various temperatures for Au/n-GaAs/GaAs structure.

The expression for the interface state density as deduced by Card and Rhoderick [3] is reduced to

$$N_{SS}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_S}{W_D}\right] \quad (7)$$

where ε_s and ε_o are the permittivity of the insulator layer and the semiconductor, respectively. δ is the thickness of insulator layer and W_D is the width of the space charge region. The natural interfacial insulator layer thickness δ was obtained from 100 kHz *C-V* characteristics using the equation for insulator layer capacitance ($C_{ox}=\varepsilon_i\varepsilon_o A/\delta$) where $\varepsilon_i=3.5\varepsilon_o$ [2,15,16] and ε_o is the permittivity of free space. Furthermore, in n-type semiconductors, the energy of the interface states E_{ss} with respect to the bottom of the conduction band at the surface of semiconductor is given by:

$$E_c - E_{ss} = q(\Phi_e - V) \quad (8)$$

The energy distribution of the interface states is shown in Fig. 3. As can be seen from the Fig. 3 the increase in the interface state density from mid gap towards the bottom of conduction band is very apparent. The values of the density of interface states are on the order ~10^{13} $eV^{-1}cm^{-2}$. Similar results have been reported in the literature [2,14,17-19]. Hanselaer et al. [19] have stated that the density of interface states of a Schottky diode with the presence of an interfacial insulator layer is lower than that of Schottky barriers without an interfacial insulator layer.

The values of R_s were evaluated using a method developed by Cheung and Cheung [27] in the high current range (at high bias voltage) where the *I-V* characteristic is not linear. Now, to determine diode parameters such as *n*, Φ_{Bo} and R_s let us obtain the functions of Cheung and Cheung [29]. From Eq. (1) the following functions can be written as:

$$\frac{dV}{dln(I)} = n\frac{kT}{q} + IR_s \quad (9)$$

$$H(I) = V - n\frac{kT}{q}ln\left(\frac{I}{AA^{*}T^{2}}\right) = n\Phi_{Bo} + IR_s \quad (10)$$

where Φ_{Bo} is the barrier height obtained from data of downward curvature region in the forward bias I-V characteristics. Experimental results show that by using the forward bias *I-V* data of a given Au/n-GaAs/GaAs structure with known rectifier contact area, two linear plots namely, *dV/d(lnI)* vs. *I* and *H(I)* vs. *I,* can be generated. In Figs. 4 (a) and (b) experimental *dV/d(lnI)* vs. *I* and *H(I)* vs. *I* plots are presented different temperatures for Au/n-GaAs/GaAs structure. Eq. (9) should give straight line for the data of downward bias *I-V* characteristics.

Table 2. The obtained n, Φ_{Bo} and R_s values by different techniques for Au/n-GaAs/GaAs structure.

T(K)	I-V		dV/dln(I)-I		H(I)-I	
	n	Φ_{Bo}[eV]	n	R_s [Ω]	R_s [Ω]	Φ_{Bo}[eV]
79	3.97	0.292	2.11	767.42	756.18	0.264
110	2.91	0.403	1.73	619.04	650.07	0.280
140	2.42	0.504	1.52	599.26	577.68	0.388
170	2.02	0.576	1.07	628.91	619.00	0.491
200	1.81	0.615	1.16	583.38	578.62	0.515
230	1.52	0.669	1.10	571.51	572.98	0.553
260	1.41	0.716	1.06	566.78	568.88	0.585
290	1.30	0.757	1.05	567.95	573.13	0.609
300	1.27	0.771	1.12	547.61	556.51	0.618
320	1.20	0.796	1.11	570.00	581.63	0.633
340	1.19	0.817	1.04	568.94	578.32	0.638
360	1.14	0.848	1.18	537.19	557.46	0.654
380	1.10	0.870	1.10	532.00	555.05	0.655
400	1.01	0.893	1.03	506.07	413.45	0.698

Thus, a plot of *dV/d(lnI)* vs. *I* plot will give R_s as the slope and *nkT/q* as the y-axis intercept. The values of *n* and R_s derived from Fig. 4 (a) and are presented in Table 2. Using the *n* value determined from Eq. (9) and the data of downward curvature region in the forward bias *I-V* characteristics in Eq. (10) a plot of *H(I)* vs. *I* according to Eq.(10) will also lead a straight line (as shown in Fig.4 (b)) with y-axis intercept equal to $n\Phi_{Bo}$. The slope of this plot also provides a second way of determination the values of R_s which can be used to check the consistency of this approach. Thus, by performing different plots (Eqs. (9) and (10)) of the *I-V* data, three main diode parameters (*n*, Φ_{Bo} and R_s) are obtained and presented in Table 2.

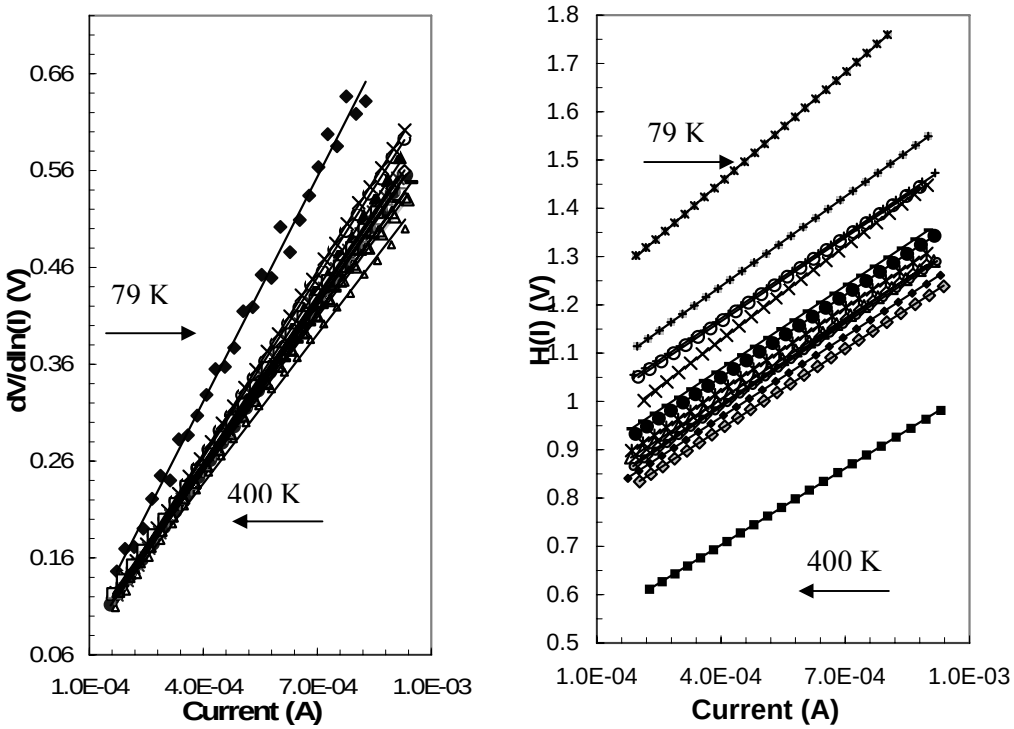

Fig. 4. Plot of (a) dV/dln(I) vs I and (b) H(I) vs I for Au/n-GaAs/GaAs structure.

Fig. 5 shows the experimental series resistance values from the forward bias semi-logarithmic I-V characteristics as a function of temperature by using a method developed by Cheung and Cheung [27].

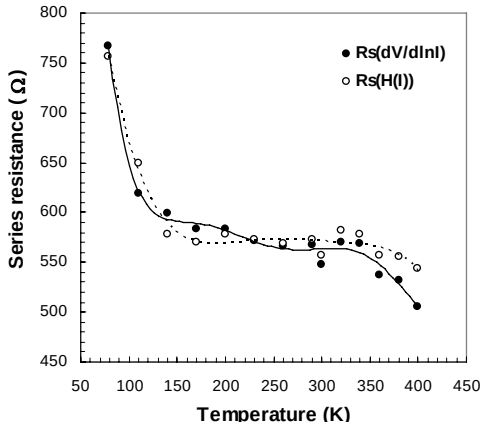

Fig. 5. The R_s vs. V plot of Au/n-GaAs/GaAs structure at various temperatures.

As can be seen in Table 2 and from Fig. 5, the values of series resistance decrease with increasing temperature but become almost constant at T ≥ 200 K. This behavior may be attributed to increase of ideality factor and lack of free carrier concentration at low temperature [30,31].

4. Conclusions

The effects of series resistance and surface states on forward and reverse bias current-voltage (*I-V*) characteristics of Au/n-GaAs/GaAs structures have been characterized and analyzed over the temperature range 79-400 K, and one of the Au/n-$Al_{0.24}Ga_{0.76}As$/GaAs structure was presented in this report. Experimental results showed non-ideal behavior for the current transport over the barrier expressed by ideality factors significantly larger than unity at lower temperatures and increasingly zero-barrier height with increasing temperature. The high value of the ideality factor *n* and the series resistance R_s are attributed to the potential drop on the interfacial insulator layer and series resistance. The downward concave

curvature of the forward bias *I-V* characteristics at sufficiently high voltages has been attributed to the presence of R_s and interfacial insulator layer, apart from the N_{ss} in equilibrium with semiconductor. The values of R_s were evaluated using a method developed by Cheung and Cheung in the high current range (at high bias voltage) where the *I-V* characteristic is not linear. It can be seen that the corrected values of the barrier height, which is including the ideality factor in the expression of reverse saturation current Io, is close agreement with the temperature coefficient of the barrier height. The density of interface states distribution profile as a function of E_c-E_{ss} obtained from *I-V* measurements decreased with increasing temperature. It was seen to appear a minimum and shifting towards the conduction band in the N_{ss} curves. The improvement obtained by the temperature effect is probably due to the thermal restructuring and reordering of the insulator-semiconductor surface. In summary, it is clear that ignoring these R_s and N_{ss} can lead to very significant errors in the analysis of electrical characteristics.

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