The determination of series resistance and interface state density distributions of Au/p-type GaAs Schottky barrier diodes

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The electronic and interface state density distribution properties obtained from current–voltage (I–V) and capacitance–voltage (C–V) characteristics of Au/p-type GaAs Schottky barrier diode (SBD) at room temperature was investigated. The (I–V)–T characteristics are analysed on the basis of thermionic emission (TE). The forward bias I–V of SBDs have been studied at room temperature. SBD parameters such as ideality factor n, series resistance (R_S) determined by Cheung's functions and Schottky barrier height, $\Phi_{bo,}$ are investigated as functions of temperature. The diode parameters such as ideality factor, series resistance and barrier heights were found as 1.76-2.16 and 2.2-1.8 Ω and 0.53–0.72 eV, respectively. The diode shows non-ideal I–V behaviour with an ideality factor greater than unity. Furthermore, the energy distribution of interface state density was determined from the forward bias I–V characteristics by taking into account the bias dependence of the effective barrier height. The results show the presence of thin interfacial layer between the metal and semiconductor.

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1. Introduction

Metal–semiconductor (MS) Schottky diodes are an essential part of virtually all semiconductor electronic and optoelectronic devices. Semiconductor devices are the basic components of integrated circuits and are responsible for the startling rapid growth of electronics industry in the past 50 years worldwide. Because there is a continuing need for faster and more complex systems for the information age, existing semiconductor devices are being studied for improvement, and new ones are being invented [1–3]. Due to technological importance of MS GaAs SBDs, a full understanding of the nature of the electrical characteristics of SBDs in this system is of great interest. Thus, SBSs have an important role for electronic technology [4–5]. Electronic properties of a Schottky diode are characterized by its barrier height and ideality factor parameters. The interface states play an important role on determination of Schottky barrier height and other characteristic parameters and these can affect device performance, stability and reliability [1-5]

In the study, the I–V characteristics of Au Schottky contacts on p-GaAs substrate were measured at room temperature. Electrical parameters such as ideality factor, barrier height series resistance and Richardson constant were extracted from forward bias I-V measurements. Thus, we examined the electronic properties of main parameters obtained from current–voltage (I–V) and capacitance–voltage (C–V) measurements and interface state density distribution properties of interface states of Au/p-GaAs SBD.

2. Experimental procedures

The semiconductor substrates used were p-type Zn-doped GaAs single crystals, with a (100) surface orientation, 300 μm thick and 2 in. diameter. The sample was ultrasonically cleaned in trichloroethylene and ethanol, etched by $H_2SO_4/H_2O_2/H_2O$=5:1:1 (weight ratio) solution for 30 s., rinsed by propylene glycol and blown with dry nitrogen gas. Immediately after surface cleaning, ohmic contacts of low resistance on the backside of the samples were formed by evaporating 1900A˚ thick Au followed by a temperature treatment at 450 C^0 for 5 min in N_2 atmosphere. After that rectifier Schottky contacts were formed on the other faces by evaporating 1900A˚ thick Au. The evaporation process was carried out in a vacuum of 1.2×10^{-6} Torr. The native oxide on the front surface of the substrate was removed in HF:H_2O (1:10) solution and finally, the wafer was rinsed in de-ionised water for 30 s before forming an organic layer on the p-type GaAs substrate. Preceding each cleaning step, the wafer was rinsed thoroughly in de-ionized water of resistivity of 18 MΩ cm.

The temperature dependence of current–voltage measurements were performed by the use of a Keithley 220 programmable constant current source, a Keithley 614 electrometer at room temperature using a temperature-controlled Janes vpf-475 cryostat, which enables us to make measurements at room temperature. The sample temperature was always monitored by using a copper-constantan thermocouple close to the sample and measured with a dmm/scanner Keithley model 199 and a Lake Shore model 321 auto-tuning temperature controllers

with sensitivity better than ± 0.1K. All measurements were carried out with the help of a microcomputer through an IEEE-488 ac/dc converter card.

3. Results and discussion

Fig. 1 shows the experimental semi-log I-V characteristic of the Au/p-GaAs SBD at room temperature.

$$I = I_0 \exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(-\frac{qV}{kT}\right)\right] \quad (1)$$

where

$$I_0 = AA^*T^2 \exp\left(-\frac{q\phi_{B0}}{kT}\right) \quad (2)$$

is the saturation density, V is the definite forward-bias voltage, A is the effective diode area, k is the Boltzmann constant, T is the absolute temperature, A^* is the effective Richardson constant and equals 79.4 A $cm^{-2}K^{-2}$ for p-type GaAs [8], where Φ_{bo}(I-V) is the barrier height at zero bias (which is defined by Eq. (2)), and n is called the ideality factor, which is defined as:

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln J)}\right) \quad (3)$$

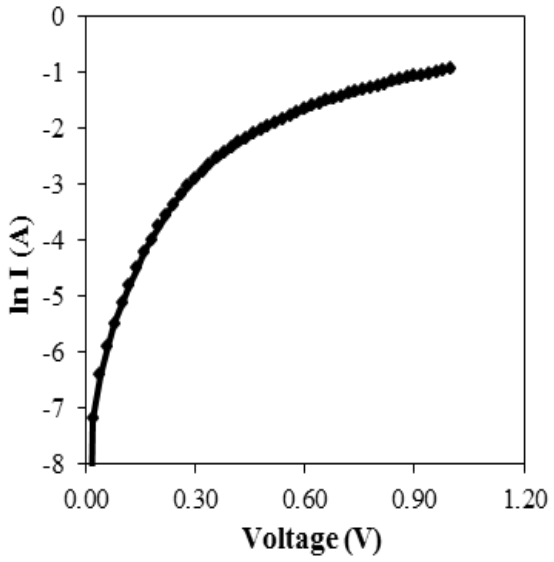

Fig. 1. The experimental forward current–voltage characteristic of the Au/p-GaAs Schottky barrier diode at room temperature.

The values of the barrier height Φ_{b0} and the ideality factor n of the Au/p-GaAs SBD were calculated as 0.53 eV from the extrapolated experimental saturation current, I_0= 1,36×10^{-4}, and n=1.53 from the slope of the linear region of the semilog-forward bias I–V characteristics indicating that the effect of series resistance in this region was not important, respectively [6-7].

Moreover, at high currents there is forever a deviation which has been clearly shown to depend on parameters such as the interfacial layer thickness, the interface states density and series resistance, as one would expected [9]. Furthermore, ideality factor and the series resistance were evaluated using a method developed by Cheung et al. [10]. The Cheung method is achieved by the functions.

$$\frac{dV}{d(\ln I)} = IR_s + n\left(\frac{kT}{q}\right) \quad (4)$$

$$H(I) = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{I_0}{AA^*T^2}\right) \quad (5)$$

$$H(I) = IRs + n\Phi_b \quad (6)$$

Eq. (4) should give a straight line for the data in the downward-curvature region of the forward bias I–V characteristics, where Φ_b is the BH obtained from data of downward curvature region in the forward bias I–V characteristics. The values of n obtained from the vertical axis intercepts of H(I)–I and dV/dln(I)–I curves (Fig. 2) and the values of R_s from their slopes were found as 1.76-2.16, and 2.2-1.8Ω, respectively. Thus, it can clearly be seen that there is relatively difference between the values of n obtained from the downward curvature regions of forward bias I–V plots and from the linear regions of the same characteristics. The reason of this difference can be attributed to the existence of effects such as the series resistance and the bias dependence of the Schottky barrier height according to the voltage drop across the interfacial layer and change of the interface states with bias in this concave region of the I–V plot. The larger value of ideality factor indicates a bias dependent barrier height which may be due to a broad barrier height distribution, i.e., a laterally nonuniform interface. Additionally, tunneling contacts, parallel to the Schottky diode, may be formed on thin oxide layers around the etched window during evaporation.

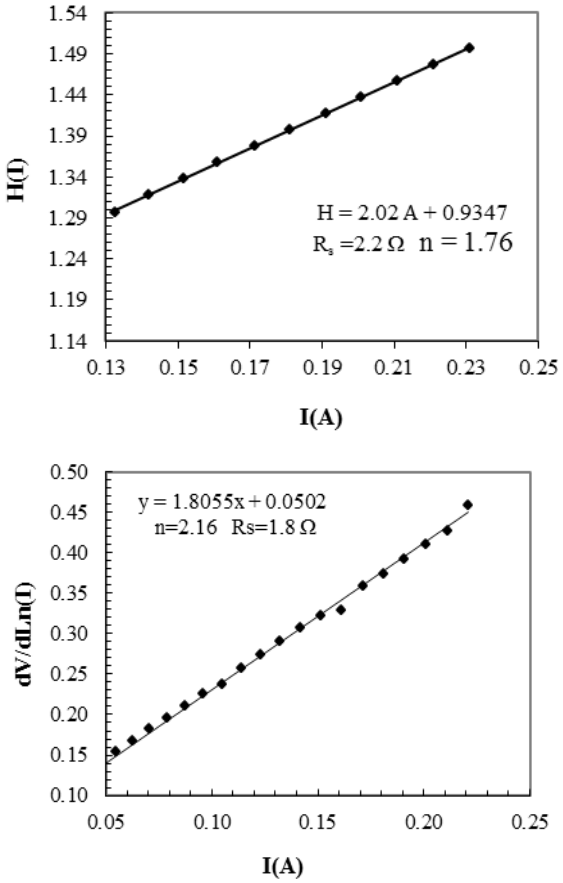

Fig. 2 The experimental H(I) vs. I and dV/dln(I) vs. I plots for the Au/p-GaAs Schottky barrier diode at room temperature.

Fig. 3 shows the C–V characteristic at room temperature measured at frequency of 1 MHz . As can be seen in figure C–V characteristic in the idealized SBDs case shows an increase in capacitance with increasing forward voltage, and the C–V characteristic has an anomalous peak. In Schottky diodes, the depletion layer capacitance can be expressed as [1,2]

$$\frac{\partial C^{-2}}{\partial V} = \frac{2}{q\varepsilon_s A^2 N_A} \tag{7}$$

or

$$C_2 = \frac{1}{n_{CV}} = \frac{2}{q\varepsilon_s N_A \left(\frac{\partial C^2}{\partial V}\right)} \tag{8}$$

where A is the area of the diode, the dielectric constant of the GaAs (=13.13 ε_0), q is the electronic charge and N_A is the acceptor concentration. The diffusion potential or built-in potential is usually measured by extrapolating $1/C^2$–V plot to the V-axis. The barrier height, Φ_{b0} (CV), from C–V measurement is defined by

$$\Phi_{b0}(\text{C-V}) = V_d - E_F - \Delta\Phi_B \tag{9}$$

where $\Delta\Phi_B$ is the image force correction and E_F is the Fermi energy According to Eq. (9), the measured barrier height Φ_{b0}(C-V) is 0.72 eV and the acceptor concentration is determined to be 2.24×10^{17} cm^{-3}. The difference between barrier heights obtained from I-V and C-V measurements is mainly due to inhomogeneities.

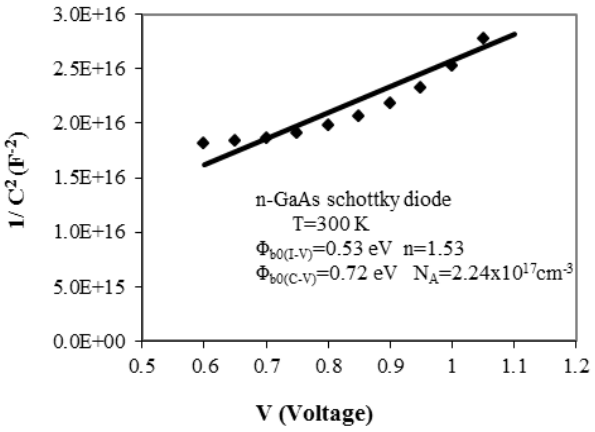

Fig. 3 Reverse bias C^{-2}–V characteristics of the Au/p-GaAs Schottky barrier diode in the frequency 1 MHz at room temperature.

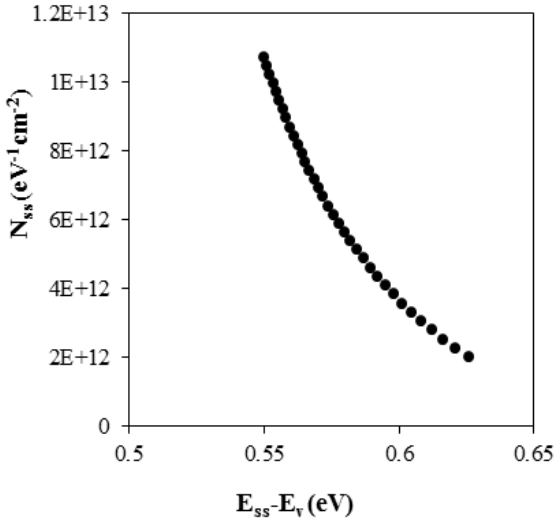

Fig. 4. Density of interface states N_{SS} as a functions of E_{SS}–E_V obtained from the I–V measurements at room temperature.

The interface state energy distribution curve of the Au/p-GaAs SBD is given in Fig. 4. For an MS diode having interface states in equilibrium with the semiconductor, the ideality factor, n becomes greater than unity as proposed by Card and Rhoderick [2] and is given by

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V)-1) - \frac{\varepsilon_s}{W_d}\right] \qquad (10)$$

where W_d is the interfacial insulator layer thickness, N_{SS} is the density of interface states, $\varepsilon_i = 13.13\,\varepsilon_0$ and $\varepsilon_0 = 8.85\times10^{-14}$Fcm^{-1} are the permittivities of the semiconductor and interfacial layer, and W_d is the thickness of insulator layer. The interfacial insulator layer thickness ($W_d = 6.3\times10^{-6}$cm) was obtained from high-frequency (1 MHz) C–V characteristic using the equation for insulator layer capacitance ($C = C_{ox} = \varepsilon' A/\delta$), and ε_0 is the permittivity of free space. Furthermore, in p-type semiconductors, the energy of the interface states with respect to the top of the conduction band at the surface of the semiconductor is given by [9,11]

$$Ess - Ev = q(\Phi e - V) \qquad (11)$$

where V is the applied voltage drop across the depletion layer and Φe is the effective barrier height. The relationship between effective barrier height, applied voltage V and the ideality factor n is given by:

$$\Phi e = \Phi_{b0} + (1 - 1/n(V)) \qquad (12)$$

The interface state density (N_{SS}) values obtained decrease with applied voltages. This confirms that the density of interface states changes with bias and each of applied biases corresponds to a position inside the GaAs gap. The value of N_{SS} obtained 1.85×10^{12}(eV)$^{-1}$cm^{-2}.

3. Conclusion

The current–voltage characteristics of Au/p-GaAs Schottky contacts were measured at room temperature. SBD parameters such as ideality factor n, the series resistance (R_S) determined by Cheung's functions and Schottky barrier height, $\Phi_{bo,}$ are investigated as functions of temperature. The diode parameters such as ideality factor, series resistance and barrier heights were found as 1.76-2.16 and 2.2-1.8 Ω and 0.53–0.72 eV, respectively. In particular, the values obtained from the C–V measurements are higher than derived from the I–V measurements as expected.

The difference between barrier heights obtained from I–V and C–V measurements is mainly due to inhomogeneities. The interface states and interfacial insulator layer at the MS interface play an important role in the determination of the characteristic parameters of the devices. The energy distribution of the interface state densities of the Au/p-GaAs diode has been determined taking into account the forward bias I–V measurements.

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