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Temperature dependence of electrical characteristics of $Au/SiO_2/n$-GaAS (MOS) structures

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Temperature dependence of capacitance-voltage (C-V) and conductance-voltage (G/w-V) characteristics of the $Au/SiO_2/n$-GaAs (MOS) structures were investigated by considering the both the interface states (N_{ss}) and series resistance (R_s) effect. Both the values of capacitance and conductance generally increase with increasing temperature. These increase in C and G/w especially at high temperatures results from the existence of interface states at SiO_2/n-GaAs interface. It is found that in the existence of R_s, the forward bias C-V curves exhibit an anamolous peak, and this peak positions shift toward from accumulation region to inversion region with increasing temperature. Also the magnitude of peak increases with increasing temperature. The values of R_s and N_{ss} were calculated by using Nicollian and Goetzberger and Hill-Coleman methods, respectively. The experimental C-V and G/w-V characteristics confirm that the R_s and N_{ss} of the MOS structure are important parameters that strongly influence the electrical characteristics of the $Au/SiO_2/n$-GaAs structures especially at high temperatures.

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1. Introduction

The metal-oxide-semiconductor (MOS) structures consist of semiconductor substrate covered by an insulator layer such as SnO_2, Si_3N_4 and SiO_2 upon which a metal electrode is deposited. Surface, interfacial insulator layer and interface properties play an important role in the electrical performance of these structures. This interfacial layer may cause interface state charges with bias due to an additional electric field in the insulator layer and influence the electrical characteristics [1-3]. The electronic states associated with the surface region were called "interface traps or surface states (D_{it} or Nss)". The reason of their existence is the interruption of the periodic lattice structure at the surface [1,3], surface preparation, dangling bonds at the semiconductor, surface formation of insulating layer and impurity concentration of semiconductor. When a voltage is applied the MOS structure, the voltage is shared by interfacial insulator layer, depletion layer and series resistance of the structure. And the magnitude of this shared voltage depends on insulator layer thickness and R_s. Therefore, the performance and reliability of these devices are especially dependent on formation of insulator layer at M/S interface. Also, the changes in the temperature interface states (Nss) and series resistance (Rs) have important effects on determination of the electrical characteristics [4-8]. Various measurement techniques for determining the N_{ss} as the high-low frequency capacitance [9,10], quasi-static capacitance [11], surface admittance [12], conductance [3,4] and Hill-Coleman methods. Among them the more important ones are Hill-Coleman method [13] and in this study the values of N_{ss} were calculated by using Hill-Coleman method.

The importance in semiconductor technology, the Si/SiO_2 and $GaAs/SiO_2$ interfaces and defects on their neighborhood have been extensively studied in literature over the long time [5-8]. There are several prepared methods of SiO_2 thin film such as thermal evaporation of oxide deposition, sputtering, sol–gel, spray deposition method, each of which had advantages and disadvantages. In this study, the insulator layer (SiO2) was coated by PECVD technique.

The main purpose in this study was to achieve a better understanding of the effects of different charge surface states and series resistance on the $Au/SiO_2/n$-GaAs structures. To do this, we have obtained the forward and reverse bias C-V and G/w-V measurements of these structures at 1 MHz with temperatures ranging from 80 K to 350 K.

2. Experimental details

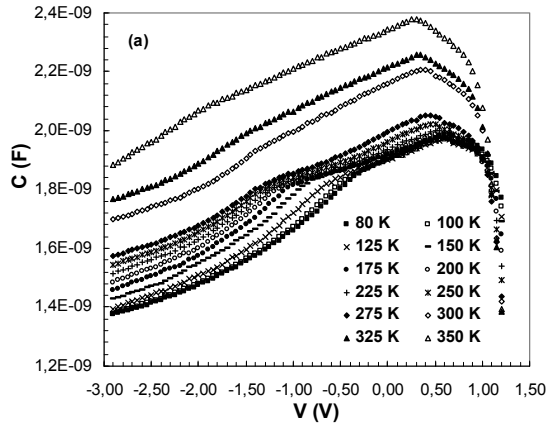
$Au/SiO_2/n$-GaAs structures were fabricated on the 5.08 cm diameter float zone (100) n-type GaAs wafer having thickness of about 350 μm with $2\text{-}3x10^{18}$ cm^{-3} carrier concentrations. For the fabrication process, the firstly GaAs wafers were dipped in ammonium peroxide for a few seconds to remove native oxide layer on the surface. Au/Ge/Ni alloy was evaporated onto the whole back side of the wafer at a pressure about 10^{-7} Torr in a

vacuum system. In order to perform the ohmic contact, wafer was sintered at 430 ^oC for 40 seconds. Insulator layer (SiO_2) with 130 Å thickness was coated on the upper surface of the GaAs by using PECVD technique. In PECVD system SiH_4 gas was used for Si source and O_2 gas used for oxygen source. After SiO_2 coating process on GaAs, the circular dots of 1 mm in diameter and 1500 Å thick high purity gold (Au) rectifying contacts were deposited with rates of about 2 Å/s onto the SiO_2 surface of the GaAs wafer through a metal shadow mask in a vacuum system in the pressure of 10^{-7} Torr. The metal layer thickness and the deposition rates were monitored with the help of quartz crystal thickness monitor.

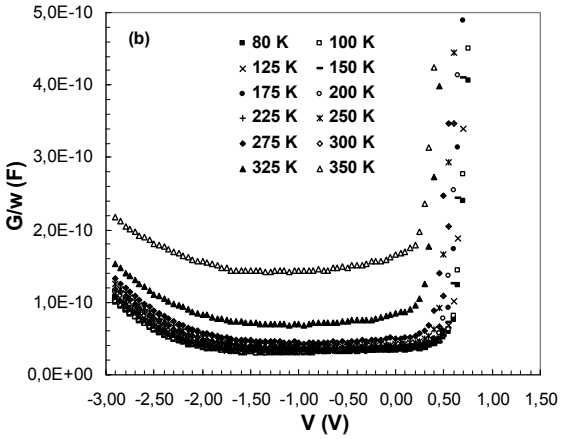
The forward and reverse bias capacitance-voltage-temperature (C-V-T) and conductance-voltage-temperature (G/w-V-T) characteristics of Au/SiO_2/n-GaAs (MOS) structure were measured in the temperature range of 80 K-350 K. The C–V and G/w-V measurements were performed at 1 MHZ by using HP 4192A LF impedance analyzer (5 Hz–13 MHz) and the test signal of 40 mV_{rms}.

3. Results and discussion

Fig. 1(a) and (b) shows the measured capacitance-voltage (C-V) and conductance-voltage (G/ω-V) characteristics of Au/SiO_2/n-GaAs (MOS) structure for different temperatures at 1 MHz, respectively. Both the C-V and G/ω-V characteristics show temperature dispersion. Generally, the C-V and G/w-V curves increases with increasing temperature. These increase in C and G/w values results from the existence of interface states at SiO_2/n-GaAs interface. In narrow band semiconductors, the charge carries are not free to move but are trapped, causing a polarization. On increasing temperature, the number of charge carries increases exponentially and thus produces further space charge polarization and hence leads to a rapid increase in the capacitance and conductance. In accumulation region; while the temperature increasing thermal energies of the majority charge carriers increase and cause dirifting inter-electrons. While these drifting is rised the series resistance (R_S), the conductance of MOS structure is increased by interface states at band gap with increasing temperature. In this reason, verifying the MOS behaviors of this structure and also indicating the presence of localized surface states at GaAs-SiO_2 interfaces, the interface states density and series resistance of this device are calculated from measured C and G/w values.



(a)



(b)

Fig.1. Capacitance-voltage (C-V) and conductance-voltage (G/w-V) characteristics of Au/SiO_2/n-GaAs structure for differenttemperatures.

The density of interface states (N_{ss}) can be derived from Hill-Coleman method [13]. According to this method, the density of interface states can be calculated by using the following equation:

$$N_{ss} = \frac{2}{qA}\frac{(G_m/\omega)_{\max}}{((G_m/\omega)_{\max}C_{ox})^2 + (1 - C_m/C_{ox})^2)} \quad (1)$$

where, A is the area of the MOS structure, w is the angular frequency, $(G_m/w)_{max}$ is the maximum measured conductance value, C_{ox} is the capacitance of insulator layer in strong accumulation region and C_m is the capacitance value, which corresponding to the $(G_m/w)_{max}$ value.

The density of interface states (N_{ss}) was shown in Table 1. The values of the N_{ss} change with increasing temperature supporting to discussion above.

Table 1. Values of N_{SS} for different temperetures determined from C_m–V and G_m/w–V measurements of Au/SiO_2/n-GaAs structure.

T (K)	V (V)	C_m (F)	G_m/w (F)	N_{SS} ($eV^{-1}cm^{-2}$)
80	0,65	$1,99x10^{-09}$	$1,24x10^{-10}$	$4,35x10^{14}$
100	0,65	$1,97x10^{-09}$	$1,45x10^{-10}$	$2,84x10^{14}$
125	0,60	$1,97x10^{-09}$	$1,01x10^{-10}$	$2,00x10^{14}$
150	0,55	$1,98x10^{-09}$	$7,18x10^{-11}$	$1,56x10^{14}$
175	0,55	$1,98x10^{-09}$	$9,17x10^{-11}$	$2,27x10^{14}$
200	0,50	$1,99x10^{-09}$	$7,80x10^{-11}$	$2,70x10^{14}$
225	0,50	$2,00x10^{-09}$	$1,09x10^{-10}$	$9,15x10^{14}$
250	0,45	$2,02x10^{-09}$	$9,17x10^{-11}$	$1,23x10^{16}$
275	0,45	$2,05x10^{-09}$	$1,41x10^{-10}$	$1,91x10^{15}$
300	0,40	$2,21x10^{-09}$	$5,03x10^{-11}$	$1,04x10^{13}$
325	0,35	$2,26x10^{-09}$	$1,77x10^{-10}$	$2,27x10^{13}$
350	0,30	$2,38x10^{-09}$	$2,36x10^{-10}$	$1,28x10^{13}$

The series resistance can be obtained from the measurements of C-V-T and G/ω-V-T curves [3];

$$R_s = \frac{G_m}{G_m^2 + \left(\omega C_m\right)^2} \qquad (2)$$

where C_m is measured capacitance and G_m is conductance values in strong accumulation region.

Fig. 2 depicts the voltage dependency of the series resistance for different temperatures at 1 MHz. As can clearly seen from the figure, the series resistance gives a peak at about 1 V, increasing with increasing temperatures. In -2 V-0,5 V bias region, the series resistance begins to constant almost voltage and temperature independent. The voltage and temperature dependency of R_S is attributed to the particular distribution of interface states density and interfacial insulator layer.

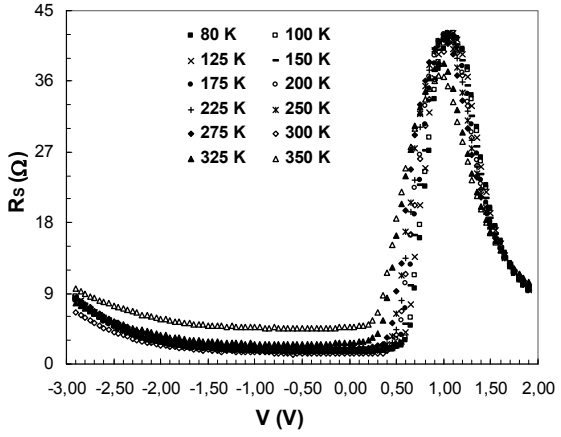


Fig. 2. Series resistance-voltage (R_S-V) characteristics of Au/SiO_2/n-GaAs structure for different temperatures.

Also, in Fig. 3, it is shown that changes in the series resistance with increasing temperature of Au/SiO_2/n-GaAs structure. Generally, from low temperature to room temperature, the series resitance increases with increasing temperature, while decreasing at above the room temperatures. While the temperature increasing until the room temperature thermal energies of the majority charge carriers increase and cause dirifting inter-electrons. These drifting is rised the series resistance (R_S) from low temperature to the room temperature. Above the room temperature, series resistance decrease with increasing temperature by contribution of interface states at band gap on conductance with increasing thermal energy.

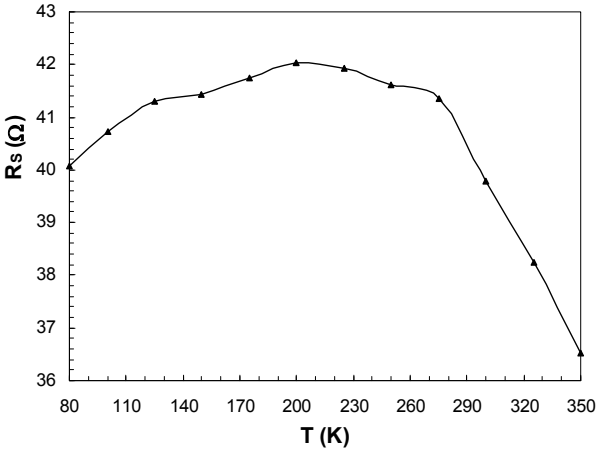


Fig. 3. Series resistance-temperature (R_S-T) characteristics of Au/SiO_2/n-GaAs structure.

4. Conclusions

In this study, the capacitance-voltage-temperature (C-V-T) and conductance-voltage-temperature (G/w-V-T) characteristics of the Au/SiO_2/n-GaAs (MOS) structures have been investigated by considering the both the interface states (N_{ss}) and series resistance (R_s) effect on C-V and G/w-V characteristics. Both the values of capacitance and conductance increase with increasing temperature. These increase in C and G/w values results from the existence of interface states at SiO_2/n-GaAs interface. Existence of R_S at accumulation region have important effect on C-V and G/w-V curves with interface states charges. While the temperature increasing until the room temperature thermal energies of the majority charge carriers increase and cause dirifting inter-electrons. These drifting is rised the series resistance (R_S) from low temperature to the room temperature. Above the room temperature, series resistance decrease with increasing temperature by contribution of interface states at band gap on conductance with increasing thermal energy. The experimental C-V and G/w-V characteristics confirm that the R_s and N_{ss} of the MOS structure are important parameters that strongly influence the electrical characteristics of the Au/SiO_2/n-GaAs structures especially at high temperatures.

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