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Studies on metal–semiconductor contacts with ZrN as metal layer

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The electrical characteristics of reactive–sputtered ZrN refractory metal nitride contacts on p-type silicon, n-type germanium and p-type gallium nitride were investigated at room temperature. It was observed that the ZrN/Si and ZrN/Ge structures exhibited rectifying characteristics, whereas ZrN/GaN showed linear current–voltage characteristics with high resistance. Rectifying parameters of Schottky barrier structure such as reverse saturation current, barrier height and depletion capacitance for low frequencies were investigated by current-voltage (I-V) and capacitance-voltage (C-V) techniques. Schottky barrier height for as-deposited ZrN/Si, ZrN/Ge structures were found to be 0.83eV and 0.61eV, respectively. Scanning electron microscopy analysis was used to study the surface morphology of the films.

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1. Introduction

Metal-semiconductor (M-S) contacts have been a subject of interest for many years. This is due to their immense use in electronics circuits like advanced VLSI/ULSI technologies. Metal-semiconductor field effect transistor technology uses the gate structure as the drain/source implantation mask and thus offers simpler-processing steps. However, processing will require that the gate material maintain a good rectifying contact with substrate. Refractory metals like W [1, 2, 3], Nb [4], Ti [5], and some of their silicides (W_5Si_3 [6, 7], $MoSi_2$ [8]) and nitrides (TiN [9], NbN [4] and WN [10, 11]) have been extensively explored for this purpose. While most of them have success to some degree, refractory metal nitrides are generally considered as very promising candidates for gate materials.

Metallization in semiconductor devices is not only for carrying current, they also play an active role in determining device parameter, as in the case of gate electrode/Schottky barrier diode [12]. Thus in present VLSI/ULSI technology, it is of fundamental interest to understand the formation of metal-semiconductor contacts (Schottky barrier, ohmic contact). The parameters which characterize such a contact, are dependent on the method used and must be considered with care.

Metal-semiconductor reactions can be grouped under two classes (a) an interaction, which results in silicide formation (Pt-Si) and (b) eutectic system, which do not form intermetallic compounds (Si-Au). Studies on Schottky barrier is interesting as electrical characteristics are extremely sensitive to conditions of the interface between the metal and semiconductor, contamination, oxide layers or metallurgical reactions, which can cause major variations in diode behaviors. Most of the metals normally used with silicon form Schottky diode. Many react with substrate to form metal silicides. Silicides formation is advantageous for contamination reduction, since critical M-S rectifying interface is within the silicon substrate where it has not been exposed to environment.

Zirconium nitride (ZrN) is a thermally stable and most widely used nitride in commercial and research applications because of its reflecting and conducting metallic behavior. It is widely known for its wear resistance, corrosion-resistance, decorative coating and good electrical-thermal conductivity. Therefore, we have fabricated ZrN/Si, ZrN/Ge and ZrN/GaN Schottky devices using ZrN as an electrode. In this paper, we report on the electrical characteristics of ZrN/Si, ZrN/Ge and ZrN/GaN Schottky devices using current–voltage (I-V) and capacitance-voltage measurements (C-V), respectively.

2. Experimental details

A 1800 Å thickness ZrN film was deposited onto different substrate like polished p-type silicon (ρ=10 Ωcm), n-type germanium (ρ=10 Ωcm) and p-type gallium nitride ($1.3\times10^{17}cm^{-3}$) by DC reactive magnetron sputtering from pure Zirconium disk (99.9%) of 100 mm diameter under optimized nitrogen partial pressure of 6×10^{-5} mbar. Optimization, fabrication and characteristic features of ZrN film have been reported [13] with annealing effects of ZrN deposited on silicon have been reported earlier [14]. The sputtering power, argon/nitrogen flow ratio, deposition time and substrate temperature were constant and was controlled to obtain the best film composition and to improve the adhesion to all these substrates. Prior to sputter deposition the sputtering target was cleaned by pre-sputtering in pure Argon for 15 min. Metal semiconductor contacts were made under the following deposition conditions at room temperature.

Ultimate base pressure 2×10^{-5}mbar	
Current	270 mA
Distance between target and substrate	11 cm
Colour of ZrN film	Golden yellow
Sputtering time	15 min
Total pressure ($Ar+N_2$)	5×10^{-4}mbar

I-V and C-V measurements were employed to characterize the Schottky devices. The electrical measurements were carried out at room temperature using digital multimeter (M-830BZ Mastech) and DM375 Multimeter (IEC 1010). Surface morphological changes like alloy penetration pits/cracks formation of ZrN films were examined by scanning electron microscopy (JEOL model JSM 5600).

3. Results and discussion

3.1. Current-voltage (I-V) characteristics

The behavior of a real Schottky diode can be modeled by the equivalent circuit as shown in Fig. 1. A series resistance Rs is associated with the bulk material in the semiconductor and ohmic back contact. Gp is the parallel conductance, which account for leakage currents. These parameters (Rs and Gp) are independent of applied voltage [15]. The effect of Gp is more important for diode with high barrier height (as high as 0.83 eV) and on reverse bias characteristics. Moreover, Werner [16] showed that the correction of the forward current for shunt current does not influence the determination of different parameter of diodes with the Schottky barrier as high as 0.83 eV. Hence Gp is neglected, with Rs=0 ohms.

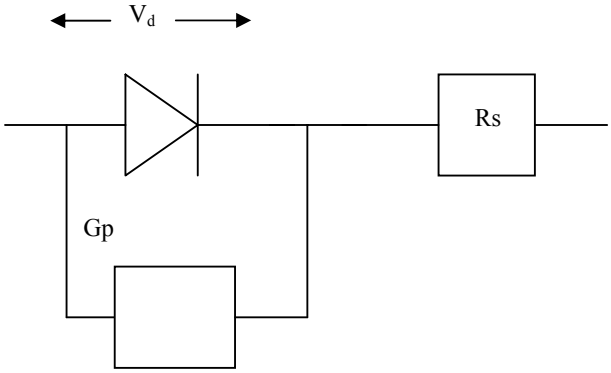


Fig. 1. Equivalent circuit of a real Schottky diode.

The relation between the current and the voltage drop across the junction Vd is given by equation 1 and equation 2.

Under reverse bias condition $I = I_s$

Where Is stands for reverse saturation current.

Under forward bias ($I=I_d$) the current I_d flowing across a rectifying metal-semiconductor contact or a P-N junction under bias V_d is usually modeled with the help of diode equation.

$$I_d = Is\left(\exp^{Vd/\eta Vt} - 1\right)$$

$$I_d = Is\left(\exp^{qV/\eta kT} - 1\right) \quad (2)$$

(under low bias voltage $\eta \geq 1$, $Vd > \eta kT/q$)

Where q/kT is inverse thermal voltage, K is Boltzmann constant, η is ideality factor, T is absolute temperature, Is is saturation current and q is electron charge.

In any Schottky diode, the current is explained by thermionic emission of the semiconductors majority carriers [17, 18]. The saturation current is usually described within the thermionic emission theory

$$Is = AA^{**}T^2\exp\left(\frac{-q\phi_b}{kT}\right) \quad (3)$$

where Is is the reverse saturation current, A** is the effective Richardson constant, A is the effective area of the diode, q is the electron charge and ϕ_b is the Schottky barrier height. (A**/A =1.1 for Ge, 0.66 for Si [18], where A** =120A/cm^2/K^2).

Fig. 2(a) and (b) shows the typical J-V characteristics of ZrN/Si and ZrN/Ge metal–semiconductor (M-S) structure. It is observed that the current increases exponentially with increase in forward bias voltage for ZrN/Si structures as shown in Fig. 2 (a). For ZrN/Ge structure, Fig. 2(b), ohmic behaviour is observed at low voltages (<1V) but at higher voltages, the junction shows a space charge condition i.e., at higher voltages the J-V characteristics are similar to ordinary P-N junction devices. The current increases linearly with respect to forward and reverse bias voltage in case of ZrN/GaN structure (Fig. 3). This characteristic feature of J-V curve confirms that ZrN/Si and ZrN/Ge are Schottky barrier diodes whereas ZrN/GaN exhibits an ohmic behavior. Schottky barrier height has been determined from equation (3), where the, reverse saturation current was obtained from I-V characteristic curve. It was found that reverse saturation current was 0.1 μA and 0.3 mA for ZrN/Si and ZrN/Ge, respectively. Barrier height was found to be 0.83 eV for ZrN/Si and 0.61 eV for ZrN/Ge. These values are close to that previously reported for the ZrN/GaAs [20] and NiTi/Si [21] structures.

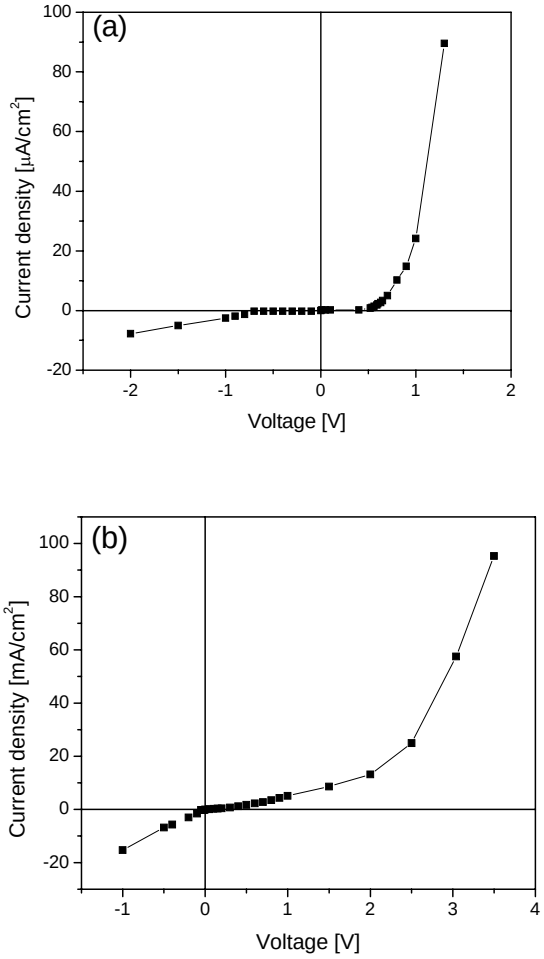


Fig. 2. J-V characteristics of (a) ZrN/Si structures and (b) ZrN/Ge structures.

Fig. 3 shows ohmic behavior with a high resistance (current is in micro range) for ZrN/GaN structure. This high resistance may be due to a very thin insulating oxide or an oxy-nitride layer between metal electrode and semiconductor, thin enough to allow only a small current to flow. Presence of such a layer shall modify the I-V characteristics of the diode. This layer would have been grown inadvertently during the sputtering process. This oxide layer is a mixture of oxygen and nitrogen interaction which is incorporated on the surface of GaN substrate, from external environment or when the sputtering chamber is exposed to atmosphere for a few minutes before loading the substrates for sputtering. This oxide layer/oxy-nitride layer may originate from diffusion and electrical activation of nitrogen with oxygen and/or nitrogen defect complexes (similar process is repeated with respect to N_2 on GaAs) [20]. Thus vacancies and voids would result on the surface of GaN substrate before ZrN metallisation.

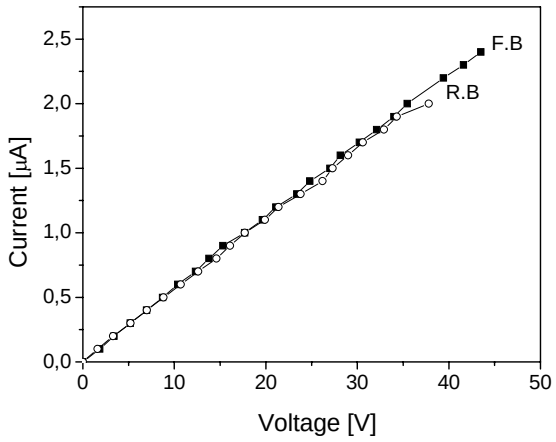


Fig. 3. The typical current –voltage characteristics of ZrN/GaN structures.

Thus at room temperature, when ZrN was deposited onto GaN substrates, it would directly reach the substrate through voids resulting in out-diffusion of Ga from GaN and in-diffusion of ZrN. These reactions shall favor a high resistance to the current flow. Here, vacancies as well as the in-diffused ZrN atoms are electrically active at room temperature only. Thus a rapid interfusion occurs which shall favour ohmic I-V characteristics (as reported for A_3B_5 compound semiconductors) [22, 23, 24]. Similar process have been reported with annealing effects [23, 24] for Sn and In in GaAs. Based on this we can conclude that the ohmic features are due to metal-semiconductor interface. ZrN diffuse distribution and possible electrical activity might have aided ohmic behavior.

3.2 Capacitance – voltage (C-V) measurement

C-V measurements of Schottky barrier play an important role in device application because the capacitance of M-S contacts is voltage dependent. We have used C-V measurements to determine only depletion capacitance and its variation with reverse bias voltage for Schottky barrier structures. The C-V measurements were made by home-built circuit at room temperature.

The plot of reverse bias voltage and depletion capacitance is shown in Fig. 4 (a) and (b) for ZrN/Si and ZrN/Ge Schottky barrier structures. Depletion capacitance is found to be in the range of 1-2.6 nF for ZrN/Si and 7-17 pF for ZrN/Ge structures, respectively. It is noticed that Schottky diodes like ZrN/GaAs, TiN/GaAs, NbN/GaAs and WN/GaAs structure showed depletion capacitance in pico farads range [20]. As reverse bias voltage is increased, the barrier height increases and depletion capacitance decreases. This is because of the presence of charged interface traps at the junction. Thus at the junction, as current increases, barrier height also increases sufficiently so that significant minority carrier injection occurs. Secondly in the direction of increasing reverse bias voltage, these interface traps change their occupancy by

the capture of leakage current holes flowing from the metal. Capture rate is more rapid than voltage sweep rate so that changes in interface trap occupancy easily follow changes in reverse voltage i.e. change in interface trap occupancy occurs with increase in reverse voltage, and stretches out each C-V curve.

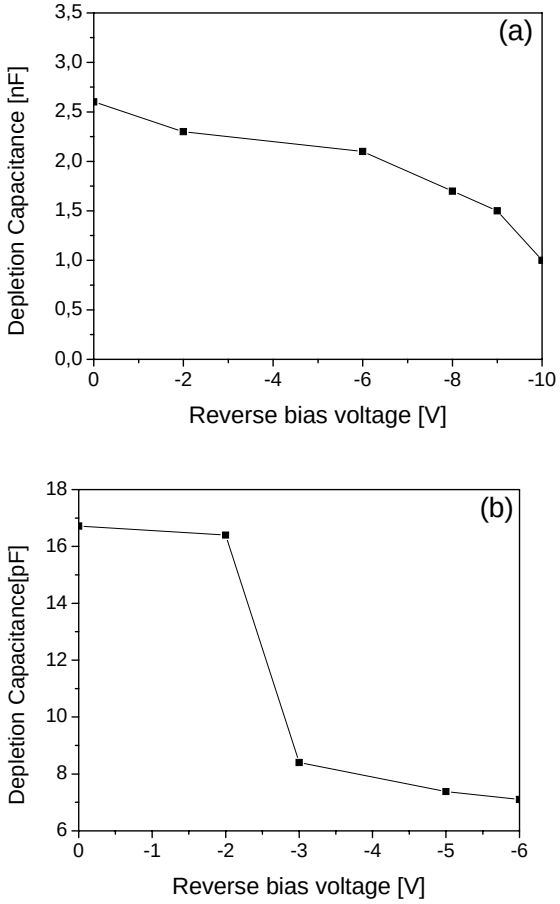
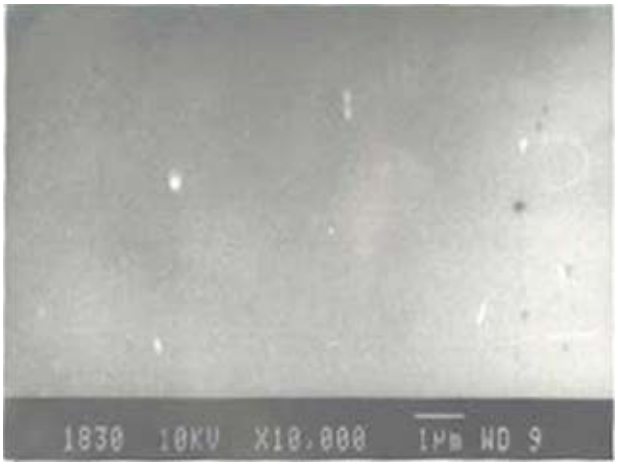


Fig. 4. C-V characteristics (Depletion capacitance versus reverse bias voltage) for (a) ZrN/Si and (b) ZrN/Ge Schottky structures.

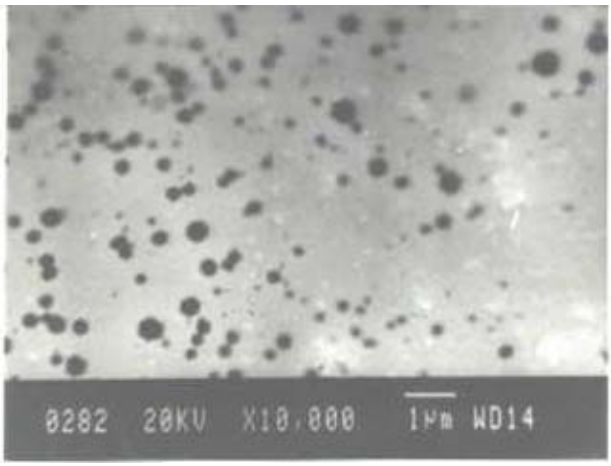
3.3 Surface morphology

In order to investigate the surface morphological changes i.e. pits/voids formation of ZrN/Si, ZrN/Ge and ZrN/GaN films were examined using scanning electron microscopy. Fig. 5 shows SEM micrographs of ZrN/Si, ZrN/Ge and ZrN/GaN. ZrN/Si films deposited at room temperature. SEM results indicate that there is no voids/pits formation for the ZrN/Si structures as shown in Fig. 5 (a). Similar features were observed for the ZrN/Ge structures as shown in Fig. 5(b). However, ZrN/GaN structure showed voids/penetration pits formation even at room temperature as shown in Fig. 5(c). Similar voids/penetration pits formation were observed in the ZrN/Si structures when annealed at 350 °C and 550 °C, which was reported earlier [25]. Annealing effects of ZrN/GaN structures are in progress.



(a) On p-type silicon substrate

(b) On n-type germanium substrate



(c) On p-type gallium nitride substrate

Fig. 5. Scanning electron micrographs of ZrN films at room temperature on (a) p - type silicon, (b) n - type germanium and (c) p-type gallium nitride substrates.

4. Summary

We have fabricated and characterized ZrN Schottky contacts on p-type silicon, n-type germanium and p-type gallium nitride substrates using I-V and C-V techniques at room temperature. The ZrN/Si and ZrN/Ge structures exhibited Schottky nature. However, ZrN/GaN structure showed linear behavior at room temperature. Barrier height was found to be 0.83 eV for ZrN/Si and 0.61 eV for ZrN/Ge, respectively. Depletion capacitance was found to be in the range of 1 to 2.6 nF for ZrN/Si and 7 to 17pF for ZrN/Ge structures, respectively. Scanning electron microscopy results confirmed that there is no formation of voids/pits in the ZrN/Si and ZrN/Ge structures. However, ZrN/GaN structure showed voids/penetration pits formation even at room temperature. Further studies are in progress to study behavior of ZrN on GaN with annealing.

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