Solution-processed coplanar top-gate ZnInSnO thin film transistors and bias stability

XIANG YANG, YANA GAO, XIFENG LI*
Key Laboratory of Advanced Display and System Application, Ministry of Education, Shanghai University, Shanghai, 200072, China

In this paper, coplanar top-gate ZnInSnO-HfAlO (ZITO-HAO) thin film transistors (TFTs) with high performance are successfully fabricated by solution process. The stability of the devices under positive stress and negative stress are investigated. The coplanar top-gate ZITO TFT devices show a high mobility of 32.8 cm^2/V•s. All the ZITO TFT devices exhibit an excellent stability. Moreover, devices under the positive and negative stress recover their original characteristics after 500s at room temperature in dark is also demonstrated. Generally, coplanar top-gate structure and the ZITO as the channel layer plays a dominant role in changing the performance of TFT devices.

(Received March 23, 2018; accepted June 14, 2019)

Keywords: Coplanar top-gate, ZnInSnO, Solution-processed

1. Introduction

Amorphous oxide thin film transistors (TFTs) have been recognized as promising candidates for next-generation display industry due to various advantages [1]. Among these amorphous oxide TFTs, which are fabricated by solution process, have attracted much attention for its simplicity, low cost and high throughput, compared with costly vacuum-based techniques [2]. So far, oxide TFTs by solution process have been generally developed as a normal bottom-gate structure including etch-stopper (ES) structures and back channel etched (BCE) [3-4]. For the BCE structure, due to the poor chemical resistance of oxide semiconductors, the patterning process (either wet etching or dry etching) of the drain/source electrode unavoidably would induce over etching of the oxide semiconductors channel layer and/or damage/exposure of the back channel [5-6]. Besides, the TFTs adopting BCE structure without passivation would face the problem of instability, because the oxygen and water in air would be absorbed at the back channel [8-9]. Such issues may be solved by adding passivation layer or using the ES configurations. But, these methods undoubtedly require additional processes which may increase the cost and complexity and also limit the shrinking of the channel length [10]. Thus, in order to overcomed the above problems, the top-gate configurations are used. The back channel of the top-gate structure would not be over etched or damaged. Furthermore, the gate insulator can also be served as the passivation for the oxide semiconductors [7]. Compared with the bottom gate TFTs, the top gate TFTs utilizing solution process might also face some problems. Since the active layer is spin-coated before the dielectric, the surface of amorphous oxide active layers would be damaged by the acidic by-product which produced during formation of dielectric oxide layer using solution technique. And it is known that the performance and stability of these TFTs are decided by the gate dielectric and its interface with the channel material. Thus, the structures, materials and process conditions must be carefully studied before fabricating the top gate TFTs. To date, there are few reports on the coplanar top gate TFTs using solution technique, let alone study their stabilities. Therefore, it is highly necessary to develop this meaningful top-gate oxide TFTs by solution technique.

In this paper, we successfully fabricate solution-processed Zn-In-Sn-O (ZITO), Hf-Al-O (HAO) TFTs with coplanar top gate configurations. Special emphasis is given on understanding the electrical bias stress effect mechanism for the solution-processed top-gate TFTs.

2. Experimental

A 0.3 M ZITO precursor was prepared by dissolving Zinc acetate dehydrate ($Zn(CH_3COO)_2 \cdot 2H_2O$, Alfa Aesar, 98%), indium chloride ($InCl_3$, Alfa Aesar, 98%) and tin chloride pentahydrate ($SnCl_4 \cdot 5H_2O$, SIGMA, 98%) in 2-methoxyethanol. Monoethanolamine (MEA) as a stabilizing agent was added. The molar ratio of Zn:In:Sn was fixed at 1:4:4. To prepare HAO solution, hafnium dichloride oxide octa-hydrate ($HfCl_2O \cdot 8H_2O$, Alfa Aesar, 98%) and aluminum-tri-sec-butoxide ($Al(OC_4H_9)_3$, Sigma Aldrich, 97%) were prepared in 2-methoxyethanol [10]. The coplanar top gate TFTs were fabricated as follows. Firstly, the synthesized ZITO solution was spin-coated at

3000 rpm for 45s on a glass substrate (0.7 mm thick, 200mm×200mm), subsequently annealed at 310 °C for 1 h. Then, repeating the spin-coating and annealing of ZITO layers twice to achieve a desired thickness (50 nm). Next, the active layer was patterned by using a wet-etch method with oxalic acid. After the patterning process of ZITO films, an ITO layer with a thickness of 50 nm was deposited on the ZITO thin film by sputtering and patterned by a wet-etch method with a mixture of phosphoric acid, acetic acid, nitric acid, and water to form source/drain electrodes. Subsequently, the HAO solution was spin-coated (45 s at 3000 rpm) and annealed (310 °C for 1 h), then the process was repeated five times to achieve dielectric layer approximately 130 nm. After the dielectric layer patterned via a wet-etch method with diluted hydrofluoric acid, a 50 nm ITO layer was deposited and patterned as gate electrodes. Finally, the TFTs were post-annealed at 500 °C for 2 hours. The channel width and channel length of the devices were 200 and 20 um, respectively. The devices were tested using the Agilent 4155C Semiconductor Parameter Analyzer to obtain the transfer and output curves. Besides, all the bias stress measurements were carried out at room temperature in the dark.

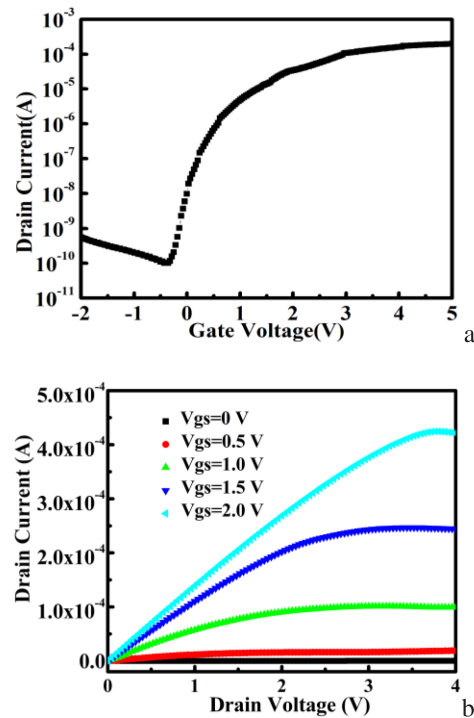

Fig. 1. (a) Transfer characteristics and gate leakage current of the fabricated top-gate TFT. (b) Output characteristics of the fabricated top-gate TFT

3. Results and discussion

Fig. 1 (a) shows the typical transfer characteristics of as-fabricated ZITO-HAO TFTs. The threshold voltage (V_{th}) is extracted from I_D-V_G curves in the saturation region by plotting the square root of the drain current versus gate voltage. The saturation mobility (μ_{sat}) is calculated from the following equation:

$$I_{DS} = (\frac{\mu_{sat} C_i W}{2L})(V_{GS} - V_{th})^2 \quad (1)$$

where C_i, W, and L are the capacitance of the gate dielectrics per unit area, the channel width and the length of the TFT, respectively.

The subthreshold swing is extracted from the linear part of the log (I_{DS}) versus V_{GS} plot. The field-effect mobility is 32.8 $cm^2V^1s^{-1}$, the subthreshold swing is about 213 mV/decade, the threshold voltage is 0.83V and the on-off drain current ratio (I_{on}/I_{off}) of TFT device is 1×10^6. Fig. 1 (b) shows the output I_D-V_D characteristics, with well-behaved current saturation. The output characteristics do not show current crowding at the beginning of the curve, which imply that the good ohmic contact between the source/drain electrodes and active layer. Besides, the series resistance at the source/drain contacts (R_{SD}) calculated by the transfer-length method (TLM) is about 4.63×10^3 Ω.

In Fig. 2, electrical-stability of the TFT devices are measured under the positive and negative bias stress for 1000 s. Bias voltage imposed on gate, drain and source during the PBS testing are (+1)/(-1) V, 1 V, 0 V, respectively. The application of a positive bias stress results in the displacement of the transfer curves in the positive direction with little change in μ_{sat}, *SS* and the I_{on}/I_{off} ratio. While, for the negative gate bias stress, it is observed that a negative shift in the threshold voltage without changing the subthreshold swing. Generally, there are two mechanisms causing instability: one is the defect creation in the channel and the other is the charge trapping between the gate dielectric and the active layer [11]. In addition, *SS* is dependent on the trap density in the active layers and at the active/insulator interface. The observed changes in the *SS* both under PBS and NBS are negligible, which indicate that no additional defects created in the channel region.

Research has also found that the metal oxides are surface sensitive to molecules in the ambient atmosphere [12]. For the BCE structure TFTs, the variation of V_{TH} can be partly attributed to oxygen or water absorption/desorption at back channel [12]. Hong et al. has reported that the desorbed/absorbed moisture or oxygen gas leaves the free electrons in the channel layers, which cause the negative V_{TH} shift of the resulting devices. However, these possible reasons explaining the instability in the bottom gate TFTs without passivation do not work

well in the top-gate TFTs. Because, in the case of top-gate TFTs, the active layers are protected by the insulator layers. Therefore, there must be other mechanisms responsible for the electrical instabilities for the top-gate TFTs.

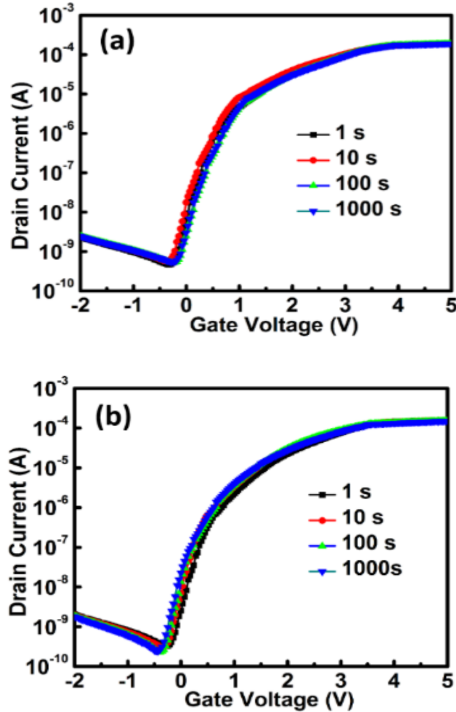

Fig. 2. Evolution of the transfer curve measured with (a) positive bias stress. (b) negative bias stress

It is known to all that the solution-processed amorphous oxide semiconductors (AOS) have inherently rich defect states, such as oxygen vacancies, metal vacancies and the like [13]. From the previous work, large number of oxygen vacancies have been found in the ZITO films [10]. In addition, donor-like and accept-like states exist at the dielectric/channel interface in other AOS TFTs [14-15]. So, it is deduced that the acceptor-like (oxygen-related and positive metal-ion-related) or donor-like (oxygen vacancy-related) defects act as the major trap sites resulting in the instabilities during the bias stress. These two defect mechanisms act in opposition, according to the results that shown in Fig. 2.

Fig. 3 shows the approximate energy diagrams under PBS and NBS. The energy level of acceptor-like states is reported at 1 eV below the conduction band edge [16]. The donor-like states sit at 2.3 eV in ZnO-based metal oxide TFTs [17]. The optical bang gap (E_g) is extracted by fitting the sharp absorption edge of the transmittance and calculated about 3.58 eV. The Fermi level (E_F) is calculated by the equation:

$$n_0 = N_c \exp[-(E_c - E_F)/kT\}] \quad (2)$$

where E_c is the minimum conduction band energy, k is the Boltzmann constant, T is the Kelvin temperature. Besides, N_c (simulated as ~10^{22}/cm^3) and no (~10^{16}/cm^3 defined by Hall measurement) are the effective density of states and the carrier concentration in the conduction band, respectively. The Fermi level is calculated at ~ 0.36 eV. The accumulated electrons near the dielectric interface are trapped by shallow acceptor-like trap states that are oxygen-related defect states [18], which results in the positive shift of the transfer curves. While it is believed that the electron-detrapping from these donor-like states (which are neutral when occupied and positive when empty) is responsible for the negative shift under NBS. In general, the neutral donor-like states have energies below the E_F. When negative voltage is applied to the gate electrode, the energy levels of trap states raise, resulting in the electron-detrapping from the neutral donor-like states. The electrons enter the channel and the threshold voltage V_{TH} decreases [17]. It is learned that both the instabilities under PBS/NBS are resulted from charge trapping/detrapping at the interface and in the ZITO channel.

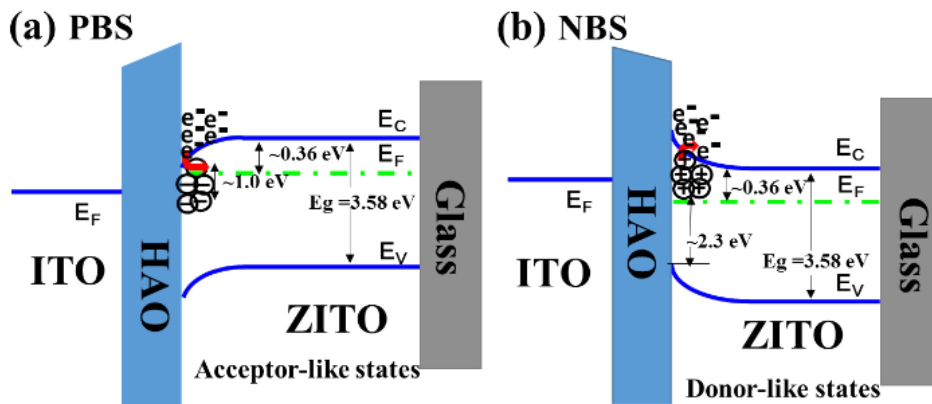

Fig. 3. Energy band diagrams under (a) positive and (b) negative bias stresses

To verify the above deduction, we also study the phenomenon of recovery for the devices. As seen in Fig. 4, the devices under tests recover their original performance after approximately 500s. The fact exhibits that these devices recover their original characteristics after a period of relaxation, without the need of any bias or thermal annealing, supports the idea that temporary interface charge trapping/detrapping may be cause the instability of device under these particular bias conditions.

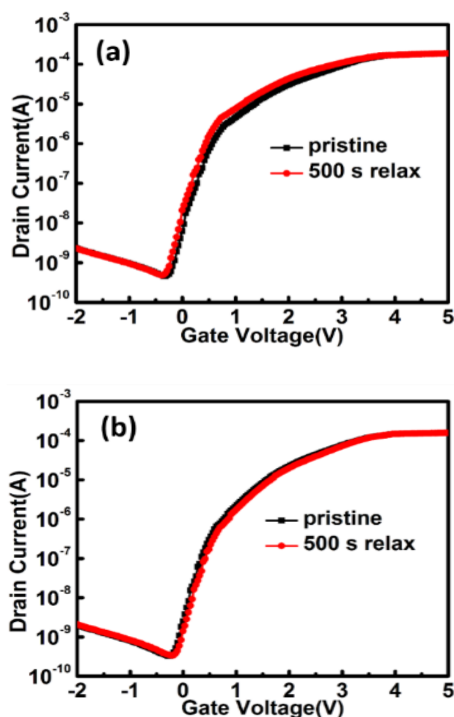

Fig. 4. The recovery of tested TFTs under (a) PBS and (b) NBS as a function of the relaxation time

4. Conclusion

In this paper, we successfully fabricated coplanar top-gate Zn-In-Sn-O (ZITO) thin-film transistors (TFTs) by sol-gel spin-coating method. The application of a positive bias stress results in the displacement of the transfer curves in the positive direction. For the negative gate bias stress, a negative shift in the threshold voltage is observed. The device under bias stress spontaneously recovered their original characteristics after a period of relaxation of 500 s at room temperature, without the aid of any thermal or bias annealing. These results indicate that the device instability may be resulted from temporary charge trapping/detrapping at the channel/insulator interface. In summary, coplanar top-gate ZITO thin-film transistors can be fabricated by solution process and it is a promising candidate structure and channel material for next generation TFTs applications.

Acknowledgements

This work is supported by the National Key Research and Development Program of China under Grant No. 2016YFB0401105, the National Natural Science Foundation of China under Grant 61674101, the Shanghai Science and Technology Commission under Grant 17DZ2291500 and the Program of Shanghai Academic/Technology Research Leader under Grant 18XD1424400. This work is also sponsored by the "Shuguang Program" supported by Shanghai Education Development Foundation and Shanghai Municipal Education Commission.

References

[1] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, Nature **432**(25), 488 (2004).
[2] B. S. Kim, Y. T. Jeong, D. Lee, T. Choi, S. H. Jung, J. W. Choi, C. Yang, K. Jo, B. J. Lee, E. Park, D. N. Kim, Y. Kim, S. Shin, Appl. Phys. Lett. **103**, 072110-1 (2013).
[3] B. Y. Su, S. Y. Chu, Y. D. Juang, H. Lee, ECS J. Solid State Sci. Technol. **2**, Q99 (2013).
[4] C. H. Kim, Y. S. Rim, H. J. Kim, J. Phys. D: Appl. Phys. **47**(38), 385104 (2014).
[5] M. Kim, J. H. Jeong, H. J. Lee, T. K. Ahn, H. S. Shin, J. S. Park, J. K. Jeong, Y. G. Mo, H. D. Kim, Appl. Phys. Lett. **90**(21), 212114-1 (2007).
[6] H. Ohara, T. Sasaki, K. Noda, S. Ito, M. Sasaki, Y. Endo, S. Yoshitomi, J. Sakata, T. Serikawa, S. Yamazaki, Jpn. J. Appl. Phys. **49**(3), 03CD02-1 (2010).
[7] C. Y. Lin, C. W. Chien, C. H. Wu, H. H. Haieh, C. C. Wu, Y. H. Yeh, C. C. Cheng, C. M. Lai, M. J. Yu, IEEE Trans. Electron Devices. **59**, 1701 (2012).
[8] J. F. Conley, IEEE Tran. Device Mater. Reliab. **10**, 460- (2010).
[9] K. H. Lee, J. S. Jung, K. S. Son, J. S. Park, T. S. Kim, R. Choi, J. K. Jeong, J. Y. Kwon, B. Koo, S. Lee, Appl. Phys. Lett. **95**, 232106-1 (2009).
[10] X. F. Li, L. Y. Zhu, Y. N. Gao, J. H. Zhang, IEEE Trans. Electron Devices **62**, 875 (2015).
[11] M. J. Powell, C. van Berkel, I. D. French, D. H. Nichols, Appl. Phys. Lett. **51**(16), 1242 (1987).
[12] H. W. Lee, B. S. Yang, Y. J. Kim, A. Y. Hwang, S. Oh, J. H. Lee, J. K. Jeong, H. J. Kim, IEEE Trans. Electron Devices **61**, 3191 (2014).
[13] Y. Jeong, C. Bae, D. Kim, K. Song, K. Woo, H. Shin, G. Cao, J. Moon, ACS Appl. Mater. Interfaces **2**, 611 (2010).
[14] K. Ghaffarzadeh, A. Nathan, J. Robertson, S. Kim, S.

Jeon, C. Kim, U. I. Chung, J.-H. Lee, Appl. Phys. Lett. **97**, 13 (2010).
[15] K. Nomura, T. Kamiya, M. Hirano, H. Hosono, Appl. Phys. Lett. **95**(1), 013502 (2009).
[16] A. Janotti, C. G. Van de Walle, Appl. Phys. Lett. **87**, 122102 (2005).
[17] X. Xiao, W. Deng, S. P. Chi, Y. Shao, X. He, L. Y. Wang, S. D. Zhang, IEEE Trans. Electron Devices **60**, 4159 (2013).
[18] W. T. Chen, S. Y. Lo, S. C. Kao, H. W. Zan, C. C. Tsai, J. H. Lin, C. H. Fang, C. C. Lee, IEEE Electron Device Lett. **32**, 1552 (2011).

*Corresponding author: lixifeng@shu.edu.cn