OPTOELECTRONICS AND ADVANCED MATERIALS – RAPID COMMUNICATIONS Vol. 1, No. 5, May 2007, p. 242 - 246

Single-chip microcomputer for application in the capacitance-frequency conversion circuit used in drop sensors

Q. SONG*, W. WU, S. ZHU, H. YAN
Automation School, Beijing University of Posts and Telecommunications, Beijing 100876, China

A capacitive drop sensor composed of the drop head and a cylindrical ring plate is designed for drop growth study. The weak capacitance signal is processed in frequency modulation circuit. The high frequency signal is measured by 8254 fast counter, which is controlled by the single-chip microcomputer 89C51, based on pulse-counting method. The counting result is stored in 89C51 first and then is transmitted to PC, through MAX232 bi-directional level transition chip, in accordance with RS-232 communication protocol. The circuit connection and the error analysis are introduced in detail. The content and flowchart of the communication protocol are presented.

(Received January 19, 2007, after revision March 27, 2007; accepted April 5, 2007)

Keywords: SCM, Capacitive sensor, Frequency, Signal processing

1. Introduction

Capacitive sensors have been widely used in dimensional and electrical measurement. They have the advantages of high sensitivity and non-contact with the measurand. The capacitive drop analysis [1,2] converts the change of drop shape during its growth to the change of the capacitance, through a specially designed capacitive sensor composed of the drop head and a cylindrical ring plate. The instant drop volume can be obtained through a simplified mathematics model.

Because of the weak variation of the capacitive signal, with its range about 0.1 pF during the drop formation from the idle capacitance of about 10pF [3], methods to obtain the capacitive signal precisely become the key factor. A frequency modulation method based on the fast counter chip 8254 controlled by the single-chip microcomputer (SCM) of 89C51 will be introduced in this paper.

2. The capacitive drop sensor

As enlightened by the cylindrical capacitive sensor, shown in figure 1(a), a special capacitive drop sensor is designed to study the liquid properties based on drop growth monitoring, which is shown in Fig. 1(b) [4].

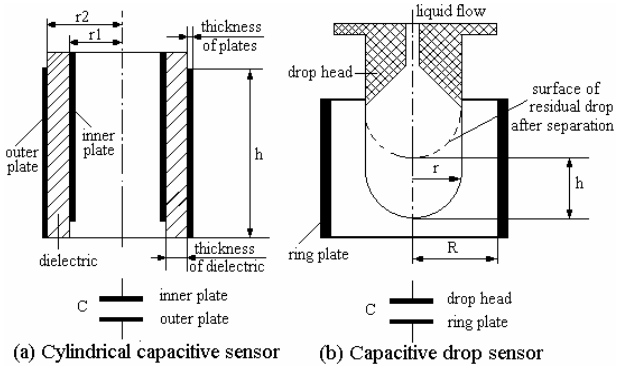

Fig. 1. The comparison between cylindrical capacitive sensor and the capacitive drop sensor.

The tested liquid is pumped into the drop head through a flexible delivery tube. The drop head is designed at its lower end with a 90°reserve cone angle to ensure that the liquid, including volatile liquids, can fully wet the end surface of the drop head [5]. The capacitive drop sensor uses the drop head as one of its plate and a cylindrical ring plate, which surrounds the drop head and the space occupied by the formed drop, as another plate. The drop, which can be seen either as an extension of the drop head plate if the liquid is highly conductive, or as a dielectric material if it is less conductive, changes the capacitance value along with drop growth.

To simply the mathematical model of the capacitive drop sensor, we assume that: (1) the drop is highly conductive; (2) the drop, during formation, only extends its length in the axis direction without changing its diameter; (3) edge effects are ignored. So the capacitance variation ΔC during drop growth from a residual drop

can be expressed approximately as:

$$\Delta C = \frac{2\varepsilon_0 \varepsilon_a \pi h}{\ln \frac{R}{r}} \quad (1)$$

where ε_0 and ε_a are the absolute dielectric constant of vacuum and the relative dielectric constant of the atmosphere respectively; h is the length of drop growth from a residual drop; R is the inner radius of the ring plate and r is the end radius of the drop head.

After simplification the drop volume variation V is given by:

$$V = \pi r^2 h \quad (2)$$

Then the relation between the capacitance variation ΔC and the drop volume variation V is obtained as the following:

$$V = \frac{k_0}{2\varepsilon_0 \varepsilon_a} \Delta C \quad (3)$$

where $k_0 = r^2 \ln \frac{R}{r}$.

Calculations show that variation of k_0 can be kept within 1% when r varies from 2.78-3.22 mm and within 5% when r varies from 2.52-4.36 mm. Therefore k_0 can be regarded as a constant when drops do not change very much in diameter. In this case, the drop volume is linearly related with the capacitance.

Since many liquids are not good conductors, errors will arise when using equation (3) in this case. By consideration of the effect of dielectric constant variations, equation (3) can be rewritten empirically as [1]:

$$V = \frac{k_1 (k_2 \varepsilon_l + \varepsilon_a)}{\varepsilon_0 \varepsilon_a (\varepsilon_l - \varepsilon_a)} \Delta C \quad (4)$$

where k_1, k_2 are correction coefficients related with the structural parameters of the drop head; ε_l is the relative dielectric constant of the tested liquid in the real-time environment. When $r = 3mm$, $k_1 = 11.23 \times 10^{-6} m^2$ and $k_2 = 0.185$ [1].

3. Signal processing circuit

Frequency modulation (FM) is widely used in capacitance measurement. Fig. 2 is its block diagram.

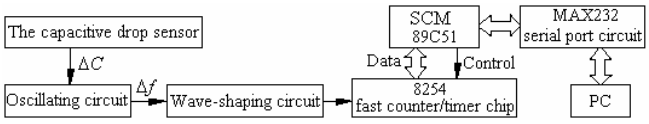

Fig. 2. The block diagram of capacitive signal processing circuit.

The capacitive signal from the drop sensor is changed into the frequency signal through a precision oscillating circuit. After wave-shaping by the LM311 comparator, the frequency signal is measured by the 8254 fast counter, which is controlled by the 89C51 microcomputer, using pulse-counting method.

The counting result is stored in 89C51 first and then is transmitted to PC, in accordance with RS-232 communication protocol between a programmable full-duplex serial port communication interface in 89C51 and an asynchronous communication adapter with its core of INS 8250 in PC. MAX232 is chosen for bi-directional level transition.

3.1 Oscillating circuit

Fig. 3 shows the MAX038 oscillating circuit. MAX038 chip is a high-frequency and precision function generator producing accurate triangle, sawtooth, sine, square and pulse waveforms. The output frequency can be controlled over a frequency range of 0.1Hz to 20MHz. When V_{FADJ} =0V as shown in Fig. 3, the fundamental output frequency (f_0) is given by the formula [6]:

$$f_o(MHz) = \frac{2 \times I_{IN}(\mu A)}{C_F(pF)} = \frac{2 \times 2.5}{R_{IN}(M\Omega) \times C_F(pF)} \quad (5)$$

If $R_{IN} = 100K\Omega$, the idle frequency is about 4MHz when there is no test liquid. The frequency variation is about 130 KHz during drop growth of pure water.

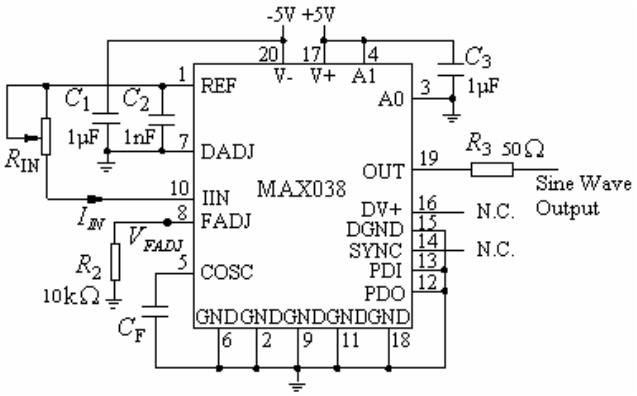

Fig. 3. MAX038 oscillating circuit.

3.2 Frequency measurement circuit

There are two ways for frequency measurement in principle: by frequency response characteristics such as resonance method, and by comparison between the standard frequency and tested frequency such as pulse-counting method. Many integrated chips including Z480-CTC, MC6840-PTM, Intel8253/8254 and SCMs including MCS-51, 96 series, are able to realize counting function through their interior system clock and counter.

SCM 89C51 has two 16-bit timer/counters. When it is used for accumulating input pulses, the period of tested signal must be 24-times greater than the system

oscillating period [7]. If the quartz crystal with 12 MHz is employed, the maximum test frequency is 500 KHz. As mentioned above, the frequency in our research is relatively high, so 89C51 itself cannot meet the demand.

Intel8254 chip provides three independent 16-bit counters, each capable of handling clock inputs up to 8MHz. Fig. 4 is its principle. The counting unit (CE) makes descending count on the CLK pulse, from the initial value set in counting register (CR). When the counting value reduces to zero, there is an output level or pulse. GATE is a control signal, which forbids counting if it is low level.

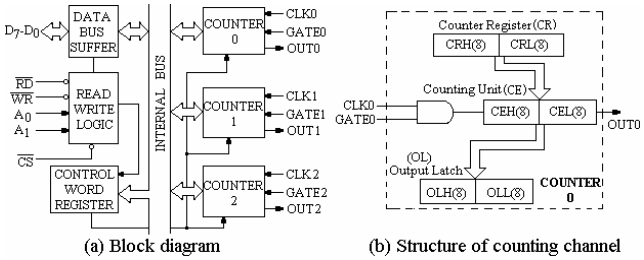

Fig. 4. The principle of Intel 8254.

If the frequency of input pulse from CLK is f_{CLK}, the positive level of GATE sustains for t_{gate}, and the number of counted pulses in the counting stage is N, as shown in Fig. 5, then we can get:

$$t_{gate} = N \times T_{CLK} = \frac{N}{f_{CLK}} \tag{6}$$

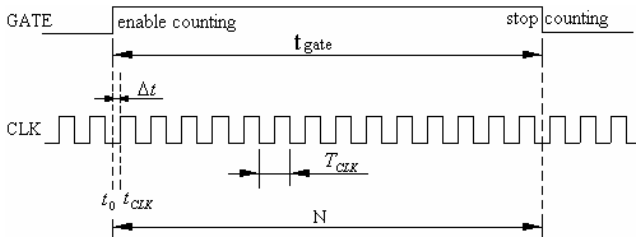

Fig. 5. Pulsing-counting method.

Commonly, the test signal is connected to GATE and the standard high-frequency pulse produced by system clock is connected to CLK. But because the frequency signal to be measured in our circuit is higher than the common system base frequency, therefore the measurand is input into CLK_0 of 8254 and is considered as the counting pulse. The gate signal ($GATE_0$) is controlled by a bi-directional I/O port (P1.1) from 89C51 and is considered as the counted pulse. Fig. 6 shows the circuit wire connection in detail.

A quartz crystal oscillator of 12MHz and two preset capacitors of 30pF are connected to XTAL1 and XTAL2 outside 89C51, to form a stable self-excited oscillator for use as the internal clock circuit. Power-on reset is automatically completed by a resistor and a capacitor connected with the RESET pin. Port 0 of 89C51 is configured to be the multiplexed low-order address bus/bi-directional data bus and port 2 emits the high-order address byte during accesses to external data memory or other functional element, such as 8254. Time-sharing operation on address and data is controlled by 74LS373 latch [7].

8-bit data bus D_0~D_7 of 8254 is connected to port 0 of 89C51 and simultaneously port 0 provides the address bus A_0, A_1 after latched by 74LS373. The chip selection is executed by the high-order address P2.7. Read-write lines are directly connected reciprocally.

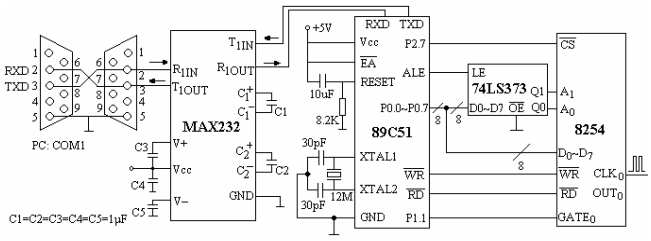

Fig. 6. Frequency measurement circuit and serial port communication circuit.

3.3 Error analysis

There is quantization error in frequency measurement using pulse-counting method. This results from the irrelevance between the hour when GATE signal enables the counter and the CLK pulse. When t_{gate} integer multiple the period of CLK pulse, quantization error reaches its maximum as ± 1 unit. Then the measured frequency can be given as:

$$f_{CLK} = \frac{N \pm 1}{t_{gate}} = \frac{N}{t_{gate}} \pm \frac{1}{t_{gate}} \tag{7}$$

The maximal relative quantization error is:

$$\frac{\Delta N}{N} = \frac{\pm 1}{N} = \pm \frac{1}{t_{gate} \times f_{CLK}} \tag{8}$$

As can be seen from equation (8), when the test f_{CLK} is certain, the longer t_{gate}, the higher the accuracy. Actually t_{gate} is limited by the 16-bit counter with its maximal count value 65536. On the other hand, if t_{gate} is fixed, the higher the frequency to be measured, the higher the accuracy. That is why the output high-frequency signal from the oscillator hasn't been divided, although the demand on frequency response of electronic elements can be reduced.

Assuming that the base frequency is 4M and t_{gate} is chosen as $1ms$, the relative error of frequency measurement is:

$$\frac{\Delta f_{CLK}}{f_{CLK}} = \frac{1/t_{gate}}{4M} = \pm\frac{1K}{4M} = \pm 0.025\% \quad (9)$$

3.4 Serial port communication between SCM and PC

89C51 has a programmable full-duplex serial port and four operation modes. Mode 1 is chosen here, viz. 10-bit asynchronous communication. The relation between baud rate and counting constant N of timer T1 is as the following:

$$N = 256 - \frac{2^{SMOD} \times f_{OSC}}{384 \times (BaudRate)} \quad (10)$$

where f_{OSC} is the oscillating frequency of 89C51 and is set as 12MHz; $SMOD$ is a constant and working parameter, which is set alternatively as 0 or 1.

Different value of $SMOD$ will cause different rounding-off error of baud rate. To ensure the communication reliability, the baud rate error should be less than 2.5%. The baud rate is chosen as 4800 here. If $SMOD = 0$, the actual baud rate after calculation is 4464.29 and its error is –6.994%. If $SMOD = 1$, the actual baud rate is 4807.07 and its error is 0.1603%. Obviously $SMOD = 1$ is more appropriate.

There is an asynchronous communication adapter with its core of INS 8250 in PC. INS 8250 is a programmable serial communication interface chip. The serial port communication between 89C51 and PC agrees with RS-232 communication protocol. MAX232 chip is chosen for bi-directional level transition between TTL level used in computer terminal and ELA level used in RS-232. The circuit connection is shown in Fig. 6.

There must be a certain mutual protocol when communication. In our study, the protocol is defined as:

(1) The communication baud rate is 4800.

(2) 89C51 waits for the enabling character "AA" from PC and then executes the measurement program.

(3) 89C51 sends to PC two block data including high 8-bit and low 8-bit data.

(4) PC sends back a verification value to 89C51 when receiving all data. Accumulative sum of high and low data is selected as the verification mode.

(5) 89C51 checks the send-back verification value and if it is right, 89C51 sends the successful termination command of character "00" and PC go on to other subsequent operation. Otherwise sends "FF" as an error command and transmits data once more.

The flowchart of serial port communication between 89C51 and PC is shown in Fig. 7.

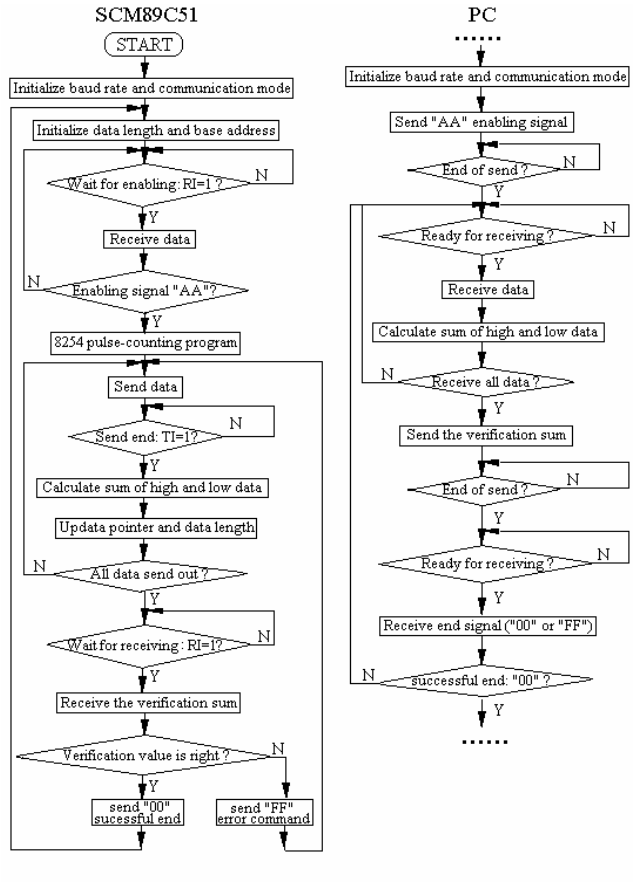

Fig. 7. The flowchart of serial port communication.

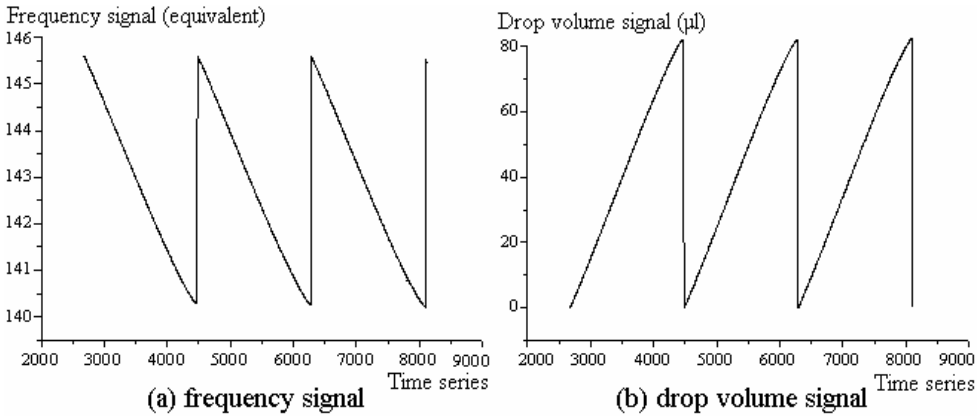

Fig. 8. The experimental graphs of pure water.

4. Experiments

Fig. 8 (a) and (b) show the experimental graphs of frequency signal and drop volume signal of the pure water. Excellent linearity between the volume and time is achieved.

5. Conclusions

During drop growth, the drop changes the capacitance value of a specially designed capacitive drop sensor composed of the drop head and a cylindrical ring plate. Drop volume can be obtained through a simplified mathematics model. Because of the weak variation of the capacitive signal in the drop formation, methods to obtain an accurate capacitive signal become the key factor.

Frequency modulation used in capacitive signal processing is relatively simple in principle and debugging. But since the tested capacitance is very low, the converted frequency is very high. The single-chip microcomputer (SCM) can be used commonly for frequency measurement, however it cannot meet the demand of our research because the maximum tested frequency is restricted by the standard oscillating period from the system quartz crystal. To solve the problem, a signal processing circuit is introduced in this paper. It has the following features:

(1) The high frequency signal is not measured through SCM 89C51 directly, but through 8254 fast counter chip, which is controlled by the SCM 89C51, based on pulse-counting method.

(2) In the pulse-counting method, the tested high-frequency signal is connected as the counted pulse (CLK) and the standard pulse produced by system clock is connected as the counting pulse (GATE). This method is reversed to the common connection method.

(3) The counting pulse (GATE) is controlled by a bi-directional I/O port from SCM 89C51. So it is not an invariable system clock and can be changed flexibly according to the practical tested frequency.

(4) The output high-frequency signal from the oscillator hasn't been divided, although this is a general processing way for reducing the demand on frequency response of electronic elements. Through error analysis in detail, frequency measurement based on pulse-counting method by fast counter chip can reach a higher accuracy, with its relative error of about ± 0.025%.

(5) The serial port communication between SCM 89C51 and PC agrees with RS-232 protocol. The baud rate is set as 4800 and its relative error is 0.16%. Accumulative sum of sending high and low data is selected as the communication verification mode.

References

[1] C. H. Wang, A. T. Augousti, J. Mason, et al. Measurement Science and Technology, **10**(1), 19-24 (1999).
[2] Song Qing, Zhang Guoxiong, Qiu Zurong, et al., **32**(1), 43-59 (2004).
[3] Song Qing, Zhang Guoxiong, Zhang Aiping, et al. Proceedings of the 2nd International Symposium on Instrumentation Science and Technology (ISIST), August 18-22, Jinan, China, Vol. **3**, 652-658 (2002).
[4] Qing Song, Zurong Qiu, Guoxiong Zhang, J. Optoelectron. Adv. Mater., **6**(4), 1213-1223 (2004).
[5] Song Qing, Zhang Guoxiong, Qiu Zurong, et al. Sensors and Materials, **16** (7), 319-334 (2004).
[6] MAXIM Corp., MAX038 high-frequency waveform generator Users Manual, 2002.
[7] He Limin, Application system design for MCS-51 Single-chip microcomputer, the publishing house of Beijing aerospace university, China. (2001).

*Corresponding author: songqing512@yahoo.com.cn