Phthalocyanine zinc thin film field-effect transistor with $SiO_2/Si_3N_4/SiO_2$ multilayer insulator

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Top-contact Phthalocyanine zinc (ZnPc) thin-film field-effect transistor (TFT) with $SiO_2/Si_3N_4/SiO_2$ multilayer as the dielectric is fabricated and investigated. $SiO_2/Si_3N_4/SiO_2$ multilayer has been prepared by magnetron sputtering. Compared to SiO_2 insulation layer device of the same thickness, the electrical characteristics of multilayer device were improved, such as the field effect mobility enhanced from 3.0×10^{-4} cm^2 /Vs to 5.8×10^{-4} cm^2 /Vs, capacitance per unit area of the gate enhanced from 10.1 nF/cm^2 to 15.3 nF/cm^2 and leakage current decreased. The $SiO_2/Si_3N_4/SiO_2$ device shows an improved performance and on-current to off-current ratio of I_{on}/I_{off} = 1.0×10^3. Atomic force microscope images of the surface of $SiO_2/Si_3N_4/SiO_2$ multilayer also have been studied.

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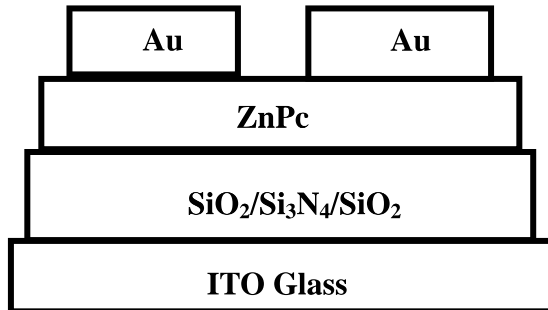
1. Introduction

Thin-film transistors(TFTs) based on organic semiconductors have received considerable attentions and increasing interests because of their potential application in displays, logic circuits, and low cost electronic devices such as smart cards due to the extraordinary electrical and mechanical properties of the small molecules [1,2]. But the operation mode of organic thin film transistor (OTFTs) cannot meet all the requirements of applications. How to improve the performance of devices is still an important problem for researchers in the field of organic electronics. As a conventional dielectric for TFTs, SiO_2 has electric stability and leakage current characteristics. However, for obtaining high carry mobility, the TFTs based on SiO_2 insulator is still a challenge due to the rather low dielectric constant of SiO_2. In recent years, Si_3N_4 has been used as OTFT gate material for its good insulated quality. It is commonly used in large scale integrated circuits in $10^{15}\Omega$ cm resistivity. Compared with SiO_2 dielectric constant (3~4), the Si_3N_4 (6~10) is larger. In TFT devices, the larger the insulating dielectric constant, the smaller thickness required of the insulation layer is [3]. Thus it increases the electric field of the semiconductor layer and reduces the device voltage, and increases the carrier mobility [4]. But the Si_3N_4 film has its shortcomings, the most prominent point is that the interface state density between Si_3N_4 film and active layer is great, when device works at threshold voltage that will reduce the stability of the thin-film transistors. In order to improve the stability, we fabricate $SiO_2/Si_3N_4/SiO_2$ multilayer insulator, making SiO_2 film contact with active layer, so as to avoid the threshold voltage drift. $SiO_2/Si_3N_4/SiO_2$ multilayer has been prepared by magnetron sputtering. We use ZnPc as active layer and study the performance of devices. ZnPc is metal complex belongs to Phthalocyanine combined with metal. The two hydrogen atoms are replaced by metal atoms in the molecule center of the plane. The metal phthalocyanine molecule has 16 π electron. The common feature of phthalocyanines is that the optical absorption spectra have two peaks named B-band and Q-band, its applications have been related to organic semiconductor, chemical sensors, electroluminescence, solar cells [5-8].

2. Experimental

The OTFT device structure used in this article is shown in Fig. 1. $SiO_2/Si_3N_4/SiO_2$ multilayer is prepared by magnetron sputtering on the ITO glass substrate, and the background vacuum is 1.2×10^{-3}Pa. The device is fabricated using Indium Tin Oxides glass as the substrate and gate electrode, with radio frequency (RF) magnetron sputtering $SiO_2/Si_3N_4/SiO_2$ layer as the gate dielectric. The deposition conditions for the Si_3N_4 and SiO_2 film are Si_3N_4 target (99.99%) and SiO_2 target(99.99%), sputtering power between 200-250W, deposition vacuum is about 1.2Pa, and we control the thickness of the film by controlling the deposit time. ZnPc thin film is prepared by vacuum deposition at the rate of 2nm/min under a pressure of 6Pa at room temperature, and the thickness of resulting films is between 30 and 45nm. OTFTs with channel length L=0.035 mm and channel width W=5 mm are fabricated by a mask. On top of this surface, gold is deposited

through this mask to give the source(S) and drain(D) electrodes. The current–voltage characteristics is calculated by transistor-detector equipment which is assembled by us.



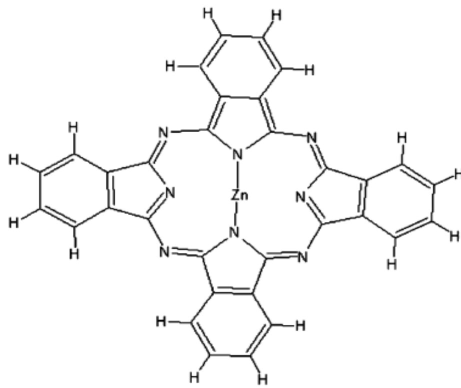


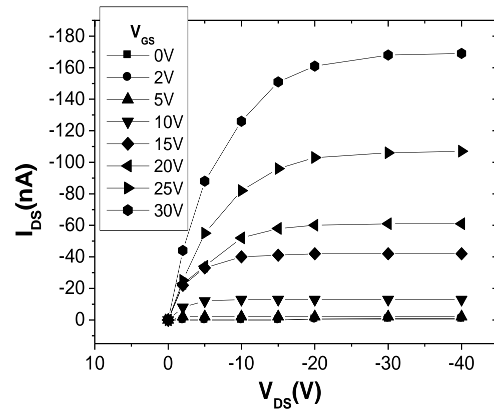
Fig. 1. Schematic structure of $SiO_2/Si_3N_4/SiO_2$ multilayer insulator thin film transistor and Molecular structures of ZnPc.

We test the $SiO_2/Si_3N_4/SiO_2$ multilayer insulator capacitance per unit area by using ZL6 automatic LCR meter. The thickness of multilayer film is tested by Korea ST2000-DLXn Apectra Thick STD-Auto device. The surface morphology of the $SiO_2/Si_3N_4/SiO_2$ multilayer is investigated by using atomic force microscopy (AFM). All experiments are carried out at room temperature.

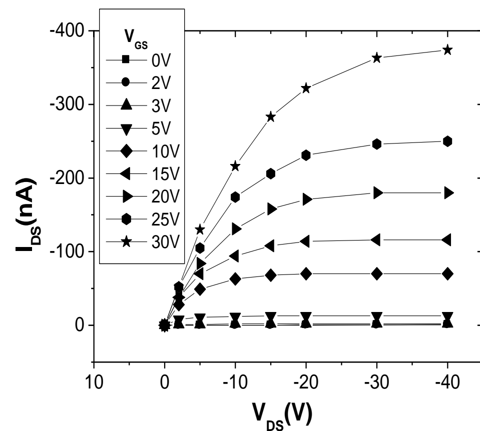
3. Results and discussion

Fig. 2 shows the typical drain current–voltage (I_{DS}–V_{DS}) curves of SiO_2 insulation layer device and $SiO_2/Si_3N_4/SiO_2$ insulation layer device at various gate voltages(V_{GS}). It can be seen that the device has a p-channel, since electrons are generated by the negative V_{GS}. The threshold voltage is negative, which indicates that the device operates in an enhancement mode. In order to compare the device performance of single insulation layer and multilayer insulation layer, the following two components are prepared:

Device a: ITO / SiO_2 (212nm) / CuPc (35nm) / Au
Device b: ITO / (SiO_2(30nm)/Si_3N_4(150nm)/SiO_2(30nm)) / CuPc (35nm) / Au



(a)



(b)

Fig. 2. (a) Drain-current characteristics of SiO_2 OTFT (b) Drain-current characteristics of $SiO_2/Si_3N_4/SiO_2$ OTFT.

The SiO_2 thickness of device 'a' is almost equal to the thickness of $SiO_2/Si_3N_4/SiO_2$ multilayer of device 'b'. When the gate and the drain voltage increases by the same, the drain current of $SiO_2/Si_3N_4/SiO_2$ multilayer device is double than that of single SiO_2 insulating layer device. The saturation mobility (μ_{sat}) could be calculated by fitting a straight line to the plot of the square root of I_{DS} versus V_{GS} (as shown in Fig. 3), according to the expression:

$$I_{DS} = \frac{WC_i}{2L}\mu(V_G - V_T)^2$$

Where C_i is the capacitance per unit area of the gate insulator, W and L are the width and length of the channel respectively. The capacitance per unit area of SiO_2 is 10.1nF/cm^2 and the capacitance per unit area of $SiO_2/Si_3N_4/SiO_2$ is 15.3nF/cm^2. The saturation mobility (μ_{sat}) of SiO_2 device and $SiO_2/Si_3N_4/SiO_2$ device are 3.0 $\times 10^{-4}$ cm^2 /Vs and 5.8$\times 10^{-4}$ cm^2 /Vs. The on/off ratio (I_{on}/I_{off}) of $SiO_2/Si_3N_4/SiO_2$ device is about 1.0×10^3.

Fig. 3 is the plot of the square root of I_{DS} versus V_{GS}

of two devices. From Fig. 3 we can see, $SiO_2/Si_3N_4/SiO_2$ multilayer insulator significantly reduces the leakage current of the device, the leakage current is relatively low, at the order of 10^{-10}A. This is because the multilayer insulator is effectively filled with the pinhole and other defect in Si_3N_4 and SiO_2 layer. Similarly, SiO_2 has filled many Si_3N_4 film layer defects, the result makes the multilayer resistance larger.

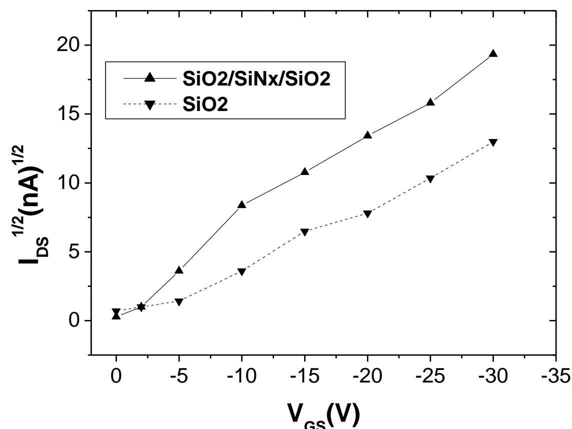


Fig. 3. The plot of the square root of I_{DS} versus V_{GS} of SiO_2 insulation layer and $SiO2/Si_3N_4/SiO_2$ insulation layer devices (V_{DS} =- 30V).

As we known, SiO_2 can be fabricated using either thermally grown or sputtering. Compared to the sputtering method, thin film that prepared by thermally grown shows smoother surface. But the sputtering method has been widely used in thin film preparation. Now we use sputtering method to fabricate $SiO_2/Si_3N_4/SiO_2$ multilayer, the multilayer of insulation that prepares between the different materials fills the defect. Therefore, sputtering process to prepare multilayer insulating layer can improve the device performance, reduce defects caused by single insulation layer. So using multilayer as gate insulator is an effective way to improve the device performance.

In the experiment, we also test the relationship between carrier mobility and the thickness of insulation layer, the relationship between leakage current and the thickness of insulation layer. The results show: thick insulating layer of insulation can make more excellent insulation properties, reduce the device leakage current, but can also cause the device to reduce the carrier mobility, increase threshold voltage. The thin insulating layer can improve the device carrier mobility, but also lead to increased device leakage current.

The surface morphology of the gate insulator is a very important factor that affects the performances of OTFTs. Fig. 4 is the 10μm×10μm atomic force microscopy image of $SiO_2/Si_3N_4/SiO_2$ surface. The influence of the insulator surface roughness to the performances of OTFTs has been investigated by several groups [9–12]. There are basically three different effects, which may contribute to the lowering of the extracted mobility with increasing roughness. The first is related to an increasing amount of trap states [13]. The other two are attributed either to grain boundaries [14]. From Fig. 4 we can see, the roughness of the $SiO_2/Si_3N_4/SiO_2$ multilayer is less than 19nm, which is still inferior as compare to the thermally grown SiO_2 insulator [15].

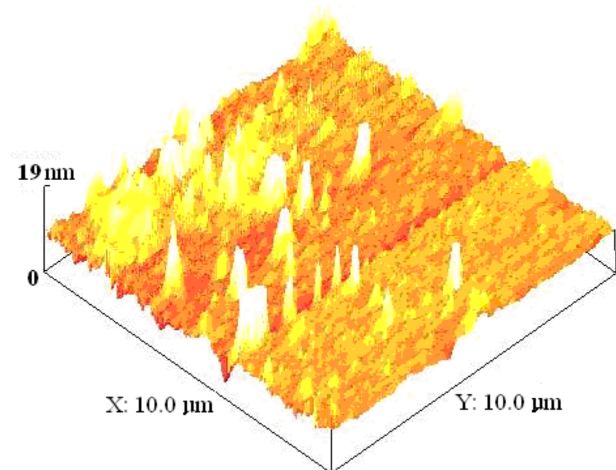


Fig. 4. 10μm×10μm atomic force microscopy image of $SiO_2/Si_3N_4/SiO_2$ surface.

4. Conclusion

In conclusion, top-contact organic thin-film transistor using ZnPc as the active layer and $SiO_2/Si_3N_4/SiO_2$ multilayer as the gate dielectric are fabricated. $SiO_2/Si_3N_4/SiO_2$ multilayer has been prepared by magnetron sputtering. Compared to single SiO_2 insulation layer, multi insulating layer devices improve carrier mobility, reduce the leakage current. Electrical parameters such as carrier mobility and on/off ratio by field effect measurement have been calculated. OTFT based on $SiO_2/Si_3N_4/SiO_2$ multilayer with a field-effect mobility of 5.8×10^{-4} cm^2 /Vs and on/off ratio of 10^3 have been obtained. AFM of the surface of $SiO_2/Si_3N_4/SiO_2$ multilayer insulating layer has been studied.

Acknowledgements

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