Optimization of annealing conditions in air for InGaZnO thin-film transistors by temperature-stress studies

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Amorphous InGaZnO (a-IGZO) thin-film transistors (TFTs) with different annealing temperatures (200 – 350 °C) were fabricated intentionally by radio frequency magnetron sputtering. The instability of a-IGZO TFTs was described by density-of-states (DOS) based on the experimentally-obtained activation energy (E_A) in temperature-stress studies and it was used to optimize the annealing conditions for a-IGZO TFTs. It was of interest to note that under annealing at 300 °C in air, the performance and stability of a-IGZO TFTs was improved significantly by increasing the annealing time to 110 min. The a-IGZO TFT annealed at 300 °C for 110 min with a field-effect mobility of 5.78 cm^2/Vs, a threshold voltage of -3.51 V, a higher on/off current ratio of 3 × 10^6 and a smaller subthreshold swing of 0.15 V/decade is very promising for driving devices in flat panel displays.

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1. Introduction

Oxide semiconductor-based thin-film transistors (TFTs) show a great potential for their application including active matrix liquid crystal display (AMLCD) and active matrix organic light emitting diode (AMOLED) [1–2]. Lack of grain boundaries, amorphous indium gallium zinc oxide (a-IGZO) TFTs with a better threshold voltage and field-effect mobility have been a very promising alternative to an amorphous silicon TFT (a-Si TFT) [3–4]. The a-IGZO film which can be fabricated at low temperatures has a wide bandgap and high transparency in the visible region. Because the ns-orbital of metal cation is larger than the 2p-orbital of oxygen anion, the a-IGZO shows high mobility although it has amorphous structure. When it comes to the fabrication of TFTs on glass or plastic substrates, the process temperature is of great importance for manufacturing devices; accordingly, the a-IGZO has great potential to replace the existing silicon based semiconductors as an active layer of the TFT backplane of the flat panels and future generation displays [5–6].

The magnetron sputtering is used widely to deposit the a-IGZO film in fabrication of the a-IGZO TFTs, which generally provides such benefits as high deposition rates and has low processing temperatures. However, lower TFT performances are shown occasionally in magnetron sputtering because of the increase in surface morphology roughness [7–9]. A decrease in the saturation mobility of TFTs, on/off current ratio, and on drain current, as well as increasing threshold voltage is caused with the interface charge trapping, scattering, and a rough surfacing [10–11]. Moreover, due to the excess of oxygen deficiency in the IGZO-sputtered films, the high conductivity is caused, which degrades the TFT performance. To overcome these problems, thermal annealing in an appropriate environment, such as O_2 or air, which could supply the oxygen component needed to compensate for the oxygen vacancies in the films, is used to improve the performance of a-IGZO TFTs [12]. Although the effect of thermal annealing on the electrical properties of a-IGZO thin films has been reported by some studies [13], the instability of a-IGZO TFTs was seldom clearly presented for this phenomenon. This paper shows the effect and the instability of a-IGZO TFTs using the extraction method of DOS with different annealing temperatures (200 – 300 °C) and considering the fabrication efficiency and cost, annealing times was limited within 110 min. It is found that the excellent electrical performance of device was shown in proper annealing condition (300 °C for 110 min) with better stability under temperature stresses.

2. Experiments

The a-IGZO TFTs were prepared on a n-Si substrate and the schematic structure of the device was shown in Fig. 1.

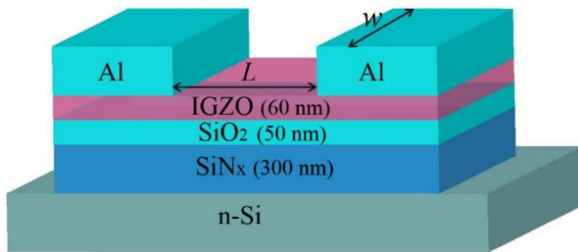

Fig. 1. The schematic structure of the device

First, the double insulator of SiO_2 (50 nm) and SiNx (300 nm) was deposited using chemical vapor deposition (CVD) technique on the Si substrate at the temperature of 350 °C and working pressure of 150 Pa (radio frequency (RF) power of 80 W) and 100 Pa (RF power of 150 W) for SiO_2 and SiNx, respectively. Next, RF magnetron sputtering was used to deposit the a-IGZO thin film of 60 nm as the active layer at the room temperature, the working pressure of 0.65 Pa and the RF power of 300 W. To remove any contamination on the target surface, pre-sputtering is performed for 10 min prior to the active layer deposition. Then, Al of about 200 nm as the source/drain (*S*/*D*) electrodes was deposited via thermal evaporation at a base pressure of 1.5 × 10^{-3} Pa. For a-IGZO TFTs, the channel width (W = 1000 μm) and length (L = 50 μm) ratio was fixed at 20. Finally, the annealing process was conducted in an air atmosphere at temperature of 200, 250, 300 and 350 °C for 20 min, and 300 °C for 20, 75 and 110 min, respectively. The measurement of electrical characteristics for a-IGZO TFTs was conducted using semiconductor parameter analyzer (Keithley, 4200-SCS) with a probe station (LakeShore, TTP4). The capacitance characteristics were measured using precision impedance analyzer (Wayne kerr 6500B).

3. Results and discussion

3.1. Optimization of annealing temperature for a-IGZO TFTs

Fig. 2 shows the transfer characteristics of the a-IGZO TFTs annealed at 200, 250, 300 and 350 °C for 20 min, respectively. As is observed, the field mobility (μ) increased significantly, while the decrease in on/off current ratio of devices was shown clearly with annealing temperature increasing. The extracted electrical parameters were listed in Table 1.

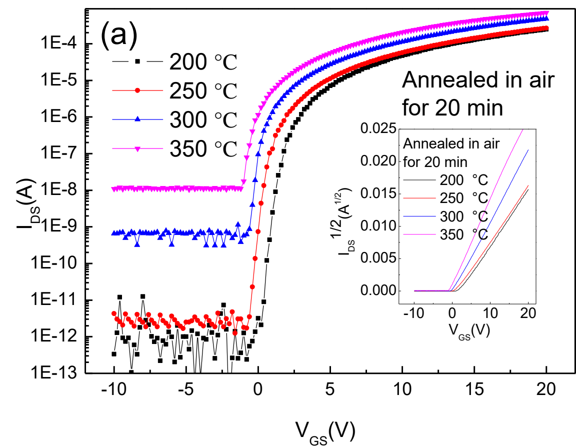

Fig. 2. The transfer characteristics of the a-IGZO TFTs annealed at 200, 250, 300 and 350 °C for 20 min, respectively. Inset: corresponding $I_{DS}^{1/2}$-V_{GS} curves

Tab. 1. List of electrical parameters of devices annealed at different temperatures

Annealing conditions (20 min)	μ (cm²/Vs)	V_{TH} (V)	on/off current ratio	*SS* (V/dec)
200 °C	5.36	2.31	1 × 10^8	0.20
250 °C	5.41	1.74	5 × 10^7	0.25
300 °C	8.32	0.58	8 × 10^5	0.30
350 °C	8.63	-3.60	1 × 10^5	0.48

The shift of threshold voltage (V_{TH}) in the negative direction caused by higher annealing temperature is deemed to be a result of the increase in the number of native defects, especially oxygen vacancies. It is known that free electrons in the ZnO-based oxide semiconductors are mainly attributed to the generation of oxygen vacancies [14]. When the oxygen atoms can preferentially leave their original sites, carriers with two electrons per oxygen vacancy are formed [15–17]. Thus, annealing at a higher temperature is expected to enhance the formation of oxygen vacancy. In a word, a higher temperature leads to more electron carriers, resulting in that V_{TH} shifts negatively as the annealing temperature increases. Besides, the a-IGZO TFT annealed at 200 °C showed a smaller *SS* compared to the device annealed at higher temperatures (250 – 350 °C). The presence of oxygen deficiencies and excess carriers caused from higher temperature were responsible for the degradation of *SS* [18–19].

Herein, V_{TH} and μ were estimated by fitting linearly the square root of the drain-source current (I_{DS}) versus the gate-source voltage (V_{GS}) ($I_{DS}^{1/2}$-V_{GS}) curve shown in Fig. 2 (inset) in the saturation region. The following equation is

the expression for the operation of a field-effect transistor in the saturation region:

$$I_{DS}=\frac{C_i\mu W}{2L}(V_{GS}-V_{TH})^2(for V_{DS}>V_{GS}-V_{TH}) \quad (1)$$

where W and L correspond to the channel width and length, respectively. C_i is the capacitance per unit area of the insulator layer, and V_{DS} and V_{GS} denote the source-drain voltage and gate-source voltage, respectively.

With the purpose of exploring the stability of devices annealed at different temperatures, the temperature-stress studies were conducted with temperatures fixed at 298, 318, 338, 358 and 378 K, respectively. At every fixed temperature value, the device in a dark environment will be measured once. Fig. 3 shows the evolution of transfer curves of a-IGZO TFTs annealed at different temperatures for 20 min under temperature stresses. The shift of V_{TH} (ΔV_{TH}) (4.28 V) for a-IGZO TFTs annealed at 200 °C was larger than that of a-IGZO TFTs annealed at 250 °C (3.42 V) 300 °C (3.32 V) and 350 °C (2.90 V), indicating that better stability was shown in a-IGZO TFTs annealed at higher annealing temperature with the same annealing time. Besides, V_{TH} shifted negatively with larger temperature stress which can be explained by the thermal activation process of the sub-threshold current. The thermally activated Arrhenius model can well explain the sub-threshold current in amorphous ZnO-based multicomponent oxide TFTs [20–21], with the basic assumption that thermally activated electrons from deep level trap sites into the conduction band move quickly toward the drain electrode because of a lateral electrical field.

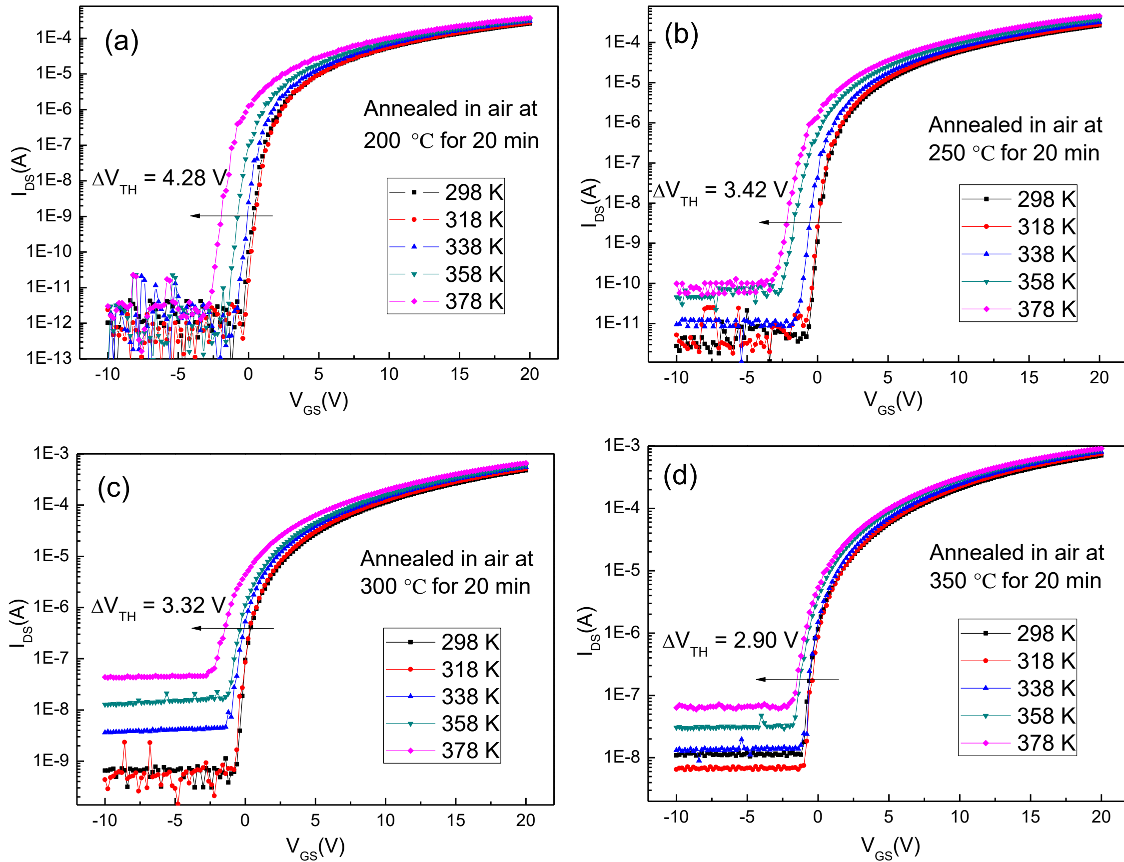

Fig. 3. The evolution of transfer curves of a-IGZO TFTs annealed at different temperatures for 20 min under temperature stresses. (a) 200 °C, (b) 250 °C, (c) 300 °C and (d) 350 °C

As is observed, the drain current is thermally activated and described by the following equation:

$$I_{DS}=I_{D0}\cdot\exp\left[-\frac{E_A(V_{GS})}{kT}\right] \quad (2)$$

where I_{D0} represents the prefactor, T is the temperature, and k is the Boltzmann constant, E_A denotes the activation energy which can be extracted from log(I_{DS}) versus $1/kT$ curves. The sample for I_{DS} - $1/T$ curves corresponding to

V_{GS} for device annealed at 200 °C for 20 min is shown in Fig. 4.

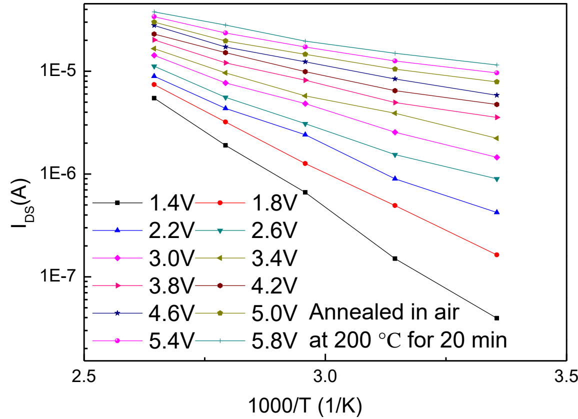

Fig. 4. The sample for I_{DS} - 1/T curves corresponding to V_{GS} for device annealed at 200 °C for 20 min

E_A-V_{GS} characteristics of a-IGZO TFTs annealed at different temperatures for 20 min can be plotted easily, as presented in Fig. 5. It is noted that the maximum E_A of 1.66 eV, 1.55 eV, 0.99 and 0.48 eV corresponded to devices annealed at 200, 250, 300 and 350 °C for 20 min, respectively. The change rate of E_A for devices annealed at 200, 250, 300 and 350 °C for 20 min was 0.75 eV $(V)^{-1}$, 0.81 eV $(V)^{-1}$, 0.84 and 0.85 eV $(V)^{-1}$, respectively. With higher annealing temperature, the device showed a faster moving E_F level with V_{GS}. It is known that the faster falling rate means the reduction in bulk and interface trap density [22]. To well clarify the distribution and density of tail states and deep states within energy bandgap in a-IGZO TFTs, the DOS of devices was calculated using the following equation:

$$g(E_A) = -\frac{\varepsilon_i}{qd_i t \dfrac{dE_A}{dV_{GS}}} \tag{3}$$

where ε_i and d_i correspond to the permittivity and thickness of gate dielectric, respectively, t denotes the thickness of active layer, and q is electron charge [22]. Fig. 5 (Inset) shows the DOS distribution as a function of the energy (E_C - E) for devices annealed at 200, 250, 300 and 350 °C for 20 min, respectively. As is seen, DOS in channel layer became smaller as the annealing temperature was elevated from 200 to 350 °C, meaning that bulk and interface trap states were strongly affected by the annealing temperature of a-IGZO active layer. It is obvious that the total DOS for device annealed at 350 °C for 20 min with faster falling rates was much smaller among all the testing devices over the entire tailing energy range extracted. Therefore, we conclude that the reduced DOS attribute to the better temperature stability at the channel layer for device annealed at 350 °C for 20 min.

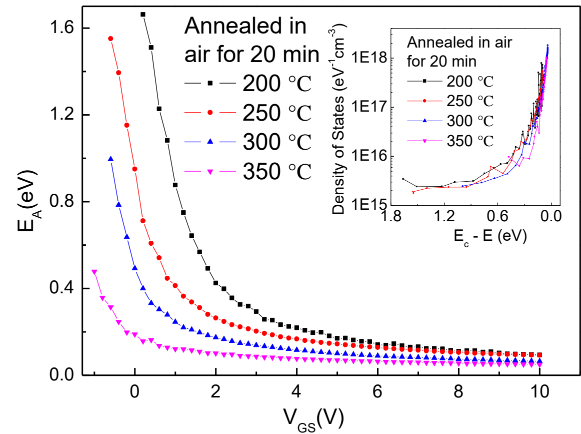

Fig. 5. E_A-V_{GS} characteristics of the a-IGZO TFTs annealed in air at 200, 250, 300 and 350 °C for 20 min, respectively. Inset: DOS distribution as a function of the energy (E_C - E) for devices annealed in air at 200, 250, 300 and 350 °C for 20 min, respectively

The stability is important for TFTs in application and a better stability help to make TFTs perform well in extreme working situations. Based on the comprehensive analysis of electronical parameters and stability for a-IGZO TFTs annealed at different temperatures above, it should be noted that the a-IGZO TFTs annealed in lower temperature and higher temperature were both not proper annealing conditions. The a-IGZO TFTs annealed in lower temperature (200 °C) with a higher on/off current ratio of up to 1×10^8 and a smaller SS of 0.20 V/decade do not show a better stability compared with other devices annealed at higher temperature. Higher annealing temperature (350 °C) can improve the stability but bring about other degradation in electronical parameters such as a larger V_{TH} (-3.60 V) and a lower on/off current ratio (1×10^5), which does not meet the requirement of the commercial products. To fabricate the a-IGZO TFTs with excellent electronical parameters and a better stability, the effect of extending annealing time at 300 °C was explored intentionally as follows.

3.2. Optimization of annealing time for a- IGZO TFTs

Fig. 6 shows the transfer characteristics of the a-IGZO TFTs annealed at 300 °C for different times. When the annealing time was extended to a longer time (110 min),

the level of off-current was improved significantly as well as *SS* while the V_{TH} shifted negatively. The extracted electrical parameters were listed in Table 2.

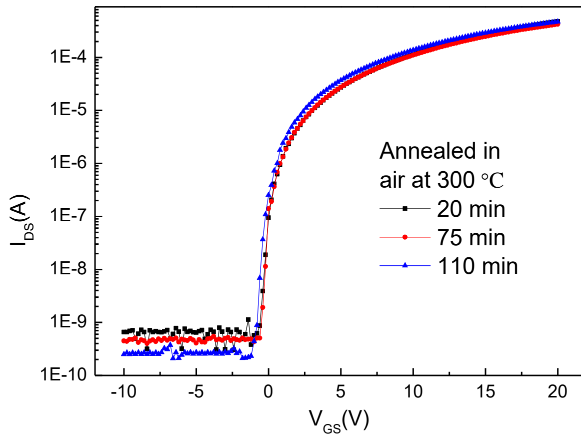

Fig. 6. The transfer characteristics of the a-IGZO TFTs annealed at 300 °C for 20, 75 and 110 min, respectively

Table 2. List of electrical parameters of TFTs annealed for different times

Annealing conditions (300 °C)	μ (cm^2/Vs)	V_{TH} (V)	on/off current ratio	*SS* (V/dec)
20 min	8.32	0.58	8×10^5	0.30
75 min	5.82	-1.18	2×10^6	0.21
110 min	5.78	-3.51	3×10^6	0.15

The evolution of transfer curves of a-IGZO TFTs annealed at 300 °C for different times under temperature stresses was shown in Fig. 7. It is found that the ΔV_{TH} of (3.32 V, 1.02 V and 0.89 V) decreased with the extension of annealing time (from 20 to 110 min) by temperature stresses, indicating that a better stability was shown in the device with longer annealing times.

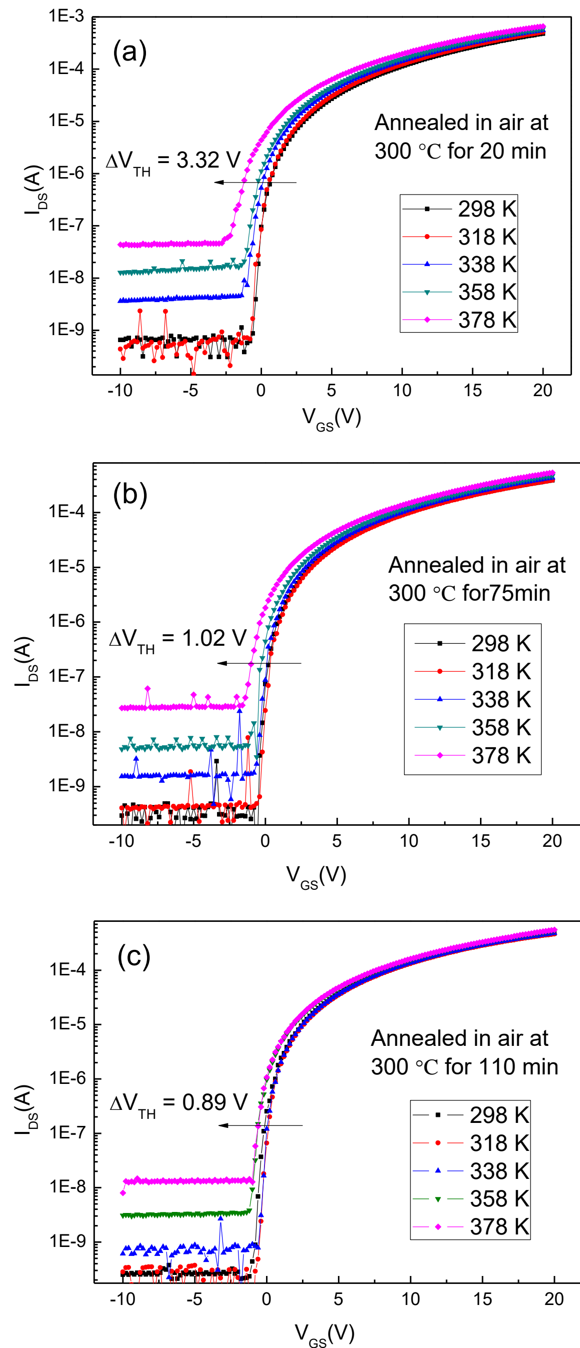

Fig. 7. The evolution of transfer curves of a-IGZO TFTs annealed at 300 °C for different times with temperature stress. (a) 20 min, (b) 75 min and (c) 110 min

E_A-V_{GS} characteristics of the a-IGZO TFTs annealed at 300 °C for different times is presented in Fig. 8. The change rate of E_A of 0.85 eV $(V)^{-1}$, 0.90 eV $(V)^{-1}$, and 1.12 eV $(V)^{-1}$ was calculated for devices annealed at 300 °C for 20, 75 and 110 min, respectively. To optimize the parameters of a-IGZO TFTs annealed at 300 °C, the DOS of a-IGZO TFTs annealed at 300 °C for different times are shown in Fig. 8 (inset). It is noted that the DOS of a-IGZO TFTs annealed in air at 300 °C was improved with

annealing time extended, indicating that the stability of a-IGZO TFTs was strengthen.

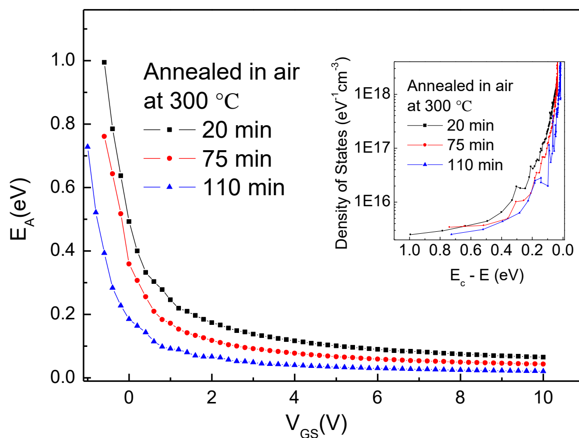

Fig. 8. E_A-V_{GS} characteristics of the a-IGZO TFTs annealed at 300 °C for 20, 75 and 110 min, respectively. Inset: DOS distribution as a function of the energy (E_C - E) for devices annealed at 300 °C for 20, 75 and 110 min, respectively

4. Conclusion

In this study, thermal annealing is very important for the electrical performance and stability of a-IGZO TFTs. Only when subjected to proper annealing temperature and time, can a-IGZO TFTs perform well, indicating that optimization of parameters is essential for the fabrication of a-IGZO TFTs. In this paper, thermal annealing was conducted to explore the excellent electrical performance and DOS was used to observe the stability of a-IGZO TFTs. The excellent performance with a better stability of device was found finally and the stability was attributed to the smaller DOS.

Acknowledgement

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