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On the temperature dependent anomalous peak and negative capacitance in Au/n-InP Schottky barrier diodes

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The temperature dependence of forward and reverse bias capacitance-voltage (C-V) and conductance-voltage (G/w-V) characteristics of Au/n-InP Schottky barrier diodes (SBDs) have been investigated in the temperature range of 80-400 K at 1 MHz. Evaluation of these experimental data reveals a peak due to series resistance in the accumulation region, and these peak positions shift toward positive bias voltage with increasing temperature. Also a negative capacitance effects has been observed in these structure. This phenomenon can be explained by considering the loss of interface charge at occupied states below Fermi level due to impact ionization. The temperature dependent C–V ,G/w–V and DLTS characteristics confirm that the R_s, N_{ss}, trap levels play an important role and strongly affect the electrical parameters of Au/n-InP SBDs. Investigation of deep level nature in Au/n-InP structure have been carried out with Sula DLTS compact system.Evaluation of two trap levels have been compared with literature.

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1. Introduction

In recent years, some investigations have reported a negative capacitance [1-5] and an anomalous peak [6-10] in the forward bias capacitance-voltage (C-V) characteristics. The change in temperature has important effects on the determination of diode parameters. Also scanning temperature depends on changing of capacitance transient, i.e. DLTS measurements, enable to characterize trap parameters such as activation energy, capture cross section and trap concentration [11]. In order to evaluate correctly some main electrical parameters such as doping concentration (N_d), barrier height (Φ_B) and series resistance (R_s), temperature dependent admittance measurements (C-V and G/w-V) are necessary to characterize of these electrical parameters correctly.

The origin anomalous peak at forward bias C-V characteristics has been ascribed to the N_{ss} by Ho et al. [12] but some investigator [9,11] reported that this peak was due to the R_s. According to Werner et al. [11], the origin of the excess capacitance also can be explained in terms of minority-carrier injection. Chathopadhyay et al. [13] have shown theoretically that the peak value of the forward bias C-V characteristics varies with both R_s and N_{ss}. Also Depas et al. [7] show that the non-equilibrium devices display a deep depletion mode (linear C^{-2} vs V) temperature dependent peaks occur in the forward bias C-V characteristics if the dominant component of the current is due to minority carriers. Also the physical mechanisms of the negative capacitance in different devices are obviously different. The observation of negative capacitance is important because they imply that an increment of bias voltage produces a decrease in the charge on the electrodes [10]. The term of negative capacitance means that the material displays an inductive behavior. The negative capacitance caused by the injection of minority carriers can be observed only at forward applied bias voltage [14].

In addition, Some electronic devices that was contacted with ohmic and schottky include in bulk traps where charges can be captured and released when the forward bias and an external a.c. oscilation voltage are applied, so important effects can be observed in devices [1,15]. Because real crystal structures have some defects that influence the electrical, mechanical, optical properties of the device. Defects that can result in reduced mobility or increased leakage current in epitaxial layers reduce device performance [11,17].

In this study, we have investigated the origin of anomalous peak and negative capacitance in the forward bias C-V-T characteristics and existence of deep levels in the Au/n-InP SBDs with DLTS scans.

2. Experimental procedure

In this study, Si doped n-type InP having thickness of 7000 A^0 was grown on n-InP(100) substrate using the VG80H solid source molecular beam epitaxy (MBE) system. Before contact process, the n-InP wafer was dipped in 5 H_2SO_4+H_20_2+ H_20 (1:1:300) solution for 1.0 min to remove surface damage layer and undesirable impurities and then in H_20+HCl solution and then followed by a rinse in de-ionized water with a resistivity of 18 M□cm. The wafer has been dried with high purity nitrogen (N_2) and inserted into the vacuum chamber immediately after the etching process then high purity gold

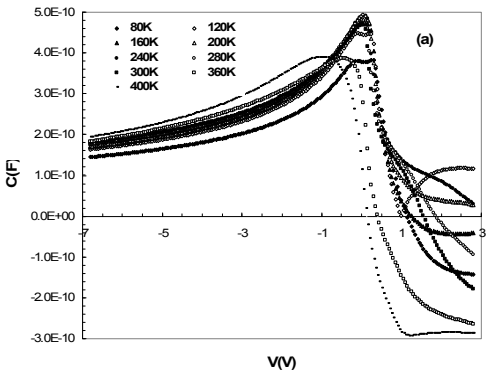
(Au) metal (99.999%) with a thickness of 1020 A^0 was thermally evaporated from the tungsten filament onto the whole back surface of the wafer in the pressure of ~ 10^{-6} Torr. The ohmic contact was formed by sintering the evaporated Au contact at 400 °C for 90 min in a flowing dry nitrogen ambient at a rate of ~2 l/min. After finishing this process, temperature was reduced to 300 ^{0}C and sample was annealled during 10 minutes. Then the sample was cooled to room temperature. To make Schottky contact on epilayer section, circular dot shaped Au Schottky contacts with a thickness of 1000 Å were formed by evaporating Au in the pressure of ~10^{-6} Torr. So Au/n-InP SBDs have been fabricated. Then the sample was removed from system and was soldered with silver pleat and then Schottky contacts were connected with conductor fiber by assistance of silver pleat.

After fabricated process of the Au/*n*-InP SBDs, temperature dependence *C-V* and *G/w-V* characteristics were measured in the temperature range of 80-400 K.

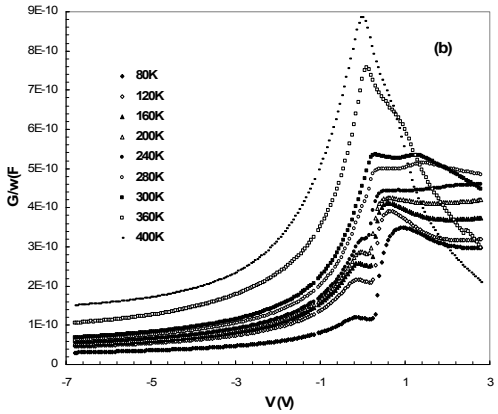
The *C–V* and *G/w-V* measurements have been performed at 1 MHz by using HP 4192A LF impedance. Experimental measurements have been carried out in the temperature range of 80-400 K using a temperature controlled Janes vpf-475 cryostat. The sample temperature has been monitored by using a copper-constantan thermocouple close to the sample and measuring with a dmm/scanner Keithley model 199 and a Lake Shore model 321 auto-tuning temperature controllers. For DLTS measurements Sula Technology compact system have been used in the 77-320K temperature range for chosen four rate windows. It is possible to detect low temperature defect (that is located about 77K) using liquid nitrogen during the DLTS measurement.

3. Results and discussion

Fig. 1 (a) and (b) show that the experimental forward and reverse bias C-V and G/w-V characteristics of Au/n-InP SBD in the temperature range of 80-400 K, respectively. As can be seen from Fig. 1(a) shows the C–V characteristics of Au/n-InP SBD, the values of capacitance give a peak in each temperature, shifting to reverse bias region with increasing temperature. The presence of the capacitance peak in the forward C–V curve is investigated by a number of experimental results on metal–insulator–semiconductor (MIS) SBDs [6-11]. Such a behavior is mainly attributed to the molecular restructuring and reordering of the interface states and series resistance. Also, Fig.1(b) shows G/w–V characteristics of the diode and exhibits the crossing of the G/w–V curves at forward bias region. Such an abnormal behavior of G/w-V can be attributed to the special distribution of interface states at metal/semiconductor interface.



(a)



(b)

Fig. 1. (a) The capacitance-voltage (C-V) and (b) conductance-voltage (G/w-V) characteristics of Au/n-InP SBD at 1 MHz at wide temperature range.

We considered that the trap charges have enough energy to escape from the traps located between metal and semiconductor interface in the InP band gap. The C^{-2}-*V* plots, which are carried out at 1 MHz and in the temperature range of 80-400 K are presented in Fig. 2.

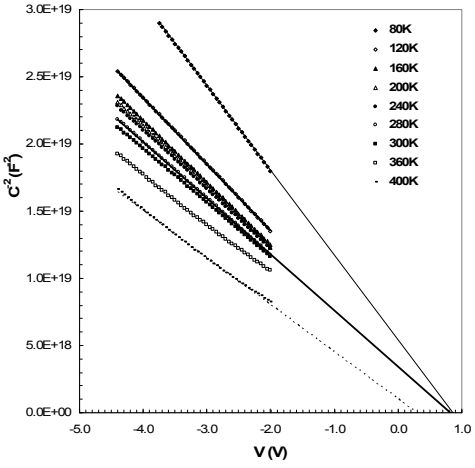


Fig. 2. The temperature dependent of C^{-2}-V plot of Au/n-InP SBD at 1 MHz.

As can be seen from Fig. 2, the C^{-2}-V plot gives a straight line in wide voltage region. For the Au/n-InP SBD, the values of carrier doping density (N_d) were determined from the slope of C^{-2}-V plots at various temperature and the barrier height values Φ_B(C-V) were calculated from using the intercept voltage (V_o=V_d-kT/q) of these plots from the relation [17],

$$\Phi_B(C\text{-}V) = V_o + kT/q + E_F - \Delta\Phi_B \quad (1)$$

where E_F, $\Delta\Phi_B$ and V_d are the energy difference between the bulk Fermi level and conductance bad edge, the image force barrier lowering and the diffusion potential, respectively. The temperature dependence of various parameters for Au/*n*-InP SBDy determined from C^{-2}-V plot are given in Table 1.

Table 1. The values of various parameters for Au/n-InP SBDs determined from C-V and G/w-V characteristics at wide temperature range.

T (K)	Vo (V)	V_d (eV)	N_d (cm^{-3})	E_F (eV)	Φ_B(C-V) (eV)
80	0.84	0.053	$2{,}93x10^{16}$	0.046	0.893
120	0.76	0.079	$3{,}30x10^{16}$	0.068	0.839
160	0.71	0.104	$3{,}55x10^{16}$	0.090	0.814
200	0.65	0.129	$3{,}77x10^{16}$	0.111	0.779
240	0.6	0.153	$4{,}02x10^{16}$	0.132	0.753
280	0.54	0.177	$4{,}30x10^{16}$	0.153	0.717
300	0.51	0.188	$4{,}62x10^{16}$	0.162	0.698
360	0.42	0.222	$5{,}13x10^{16}$	0.191	0.642
400	0.34	0.246	$5{,}28x10^{16}$	0.211	0.586

As can be seen in Table 1, the value Φ_B(C-V) decreases with temperature as

$$\Phi_B(C\text{-}V) = \Phi_{B0} - \alpha T \quad (2)$$

Here the barrier height at absolute temperature Φ_{B0} and the temperature coefficient of the barrier height a are experimentally found to be 0,96 eV and $8{,}97x10^{-4}$ eV/K, respectively. This temperature coefficient (α) of the barrier height is an obvious agreement with the reported in the literature.

One DLTS peak can only be seen at temperature where the trap emission rate is within an emission rate window. The emission rate is written by

$$e = \frac{N_0 \sigma V_{th}}{g} \exp\left(-\frac{E_a}{kT}\right) \quad (3)$$

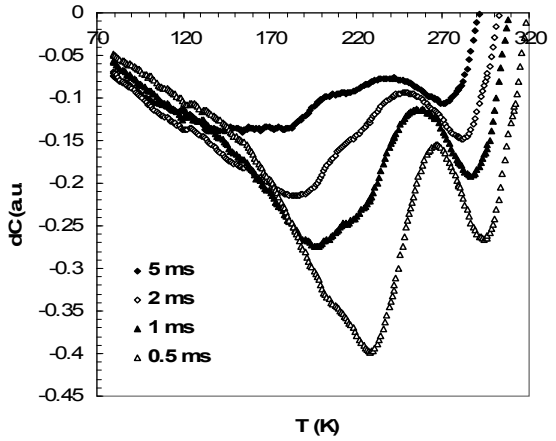
where N_o is the effective density of states, σ is the capture cross-section, V_{th} is the thermal velocity and g is the degeneracy of the level (g=2). If σ is independent of temperature, the activation energy E_a shows the energy of the trap from the band edge to which carriers are emitted. E_a can be obtained from the slope of $ln(e/T^2)$-$1/T$ plot and the capture cross-section can be calculated from intercept of this plot. Each temperature scan results in one data point on Arrhenius plot for the trap and then multiple temperature scans for enough points are required to calculate E_a, σ from Arrhenius plot.

The trap concentration is written by

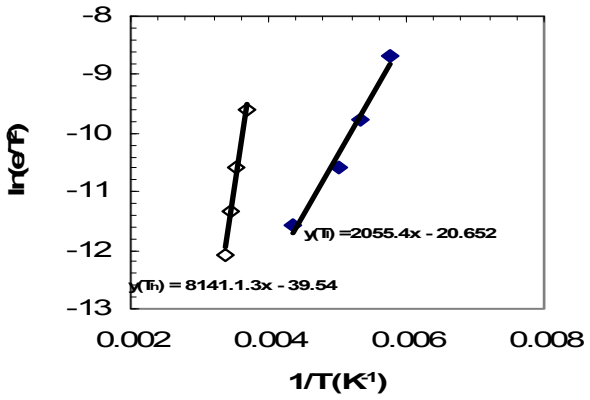
$$N_T = \frac{2\Delta C}{C}(N_D) \quad (4)$$

where ΔC is the capacitance change, i.e. data from a DLTS measurement, C is the capacitance of the diode under quiescent reverse-biased conditions, N_T trap concentration and N_D is the net donor concentration when the trap is observed.

As can be seen in Fig 3. (a), two trap levels with 0.17 eV and 0.70 eV activation energies with $3.1.10^{14}$ cm^{-3} and $1.4.10^{14}$ cm^{-3} trap concentration have been detected form DLTS scans, respectively.



(a)



(b)

Fig. 3. (a) DLTS spectra obtained in Au/n-InP SBDs. b) Arrehenius plot for Au/n-InP SBDs obtained from DLTS spectra.

For DLTS measurements four rate windows (5, 2, 1, 0.5 ms) were chosen and reverse bias, forward bias were applied as -1 V and 0.5 V, respectively in the 77-320 K temperature range. An activation energy lower than 0.2 eV has been calculated. Low activation energy can be attributed to phosphorous vacancies [18] or indium vacancies [19]. This trap can also be attributed to interface

defects due to phosphorous vacancies occupied by oxygen after surface treatment of InP [20,21].With regard to the 0.70 eV midgap defect level, its assignment to a phosphorus antisite related defect [22], this defect should be located at the middle of the InP gap[23]. Also experimental studies have reported a midgap defect level related to a phosphorus antisite in InP[24].

4. Conclusions

In this study, the effects of the interface state density (N_{ss}) and series resistance (R_s) of Au/n-InP SBDs have been investigated as a function of temperature. Experimental measurements and analyses of data show that both the capacitance and conductance were quite sensitive to temperature and voltage. The forward bias C-V characteristics show a peak due to series resistance in the accumulation region, and this peak positions shift toward positive bias voltage with increasing temperature. Also a negative capacitance effects has been observed in these structure. This phenomenon can be explained by considering the loss of interface charge at occupied states below Fermi level due to impact ionization. From DLTS results two peak have been observed in the 77-320 K temperature range. Low activation energy trap can be related to phosphorous vacancies or indium vacancies and a midgap defect is attributed to a phosphorus antisite related defect.

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