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Effects of thermal annealing on electrical and structural characteristics of Pd/n-GaN Schottky diode

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We report on the influence of annealing on the electrical and structural properties of Pd/n-GaN Schottky diode by current-voltage (I-V), capacitance-voltage (C-V), X-Ray diffraction (XRD) and Auger electron spectroscopy (AES) measurements. The Schottky barrier height of the as-deposited Pd/n-GaN was found to be 0.80 eV (*I-V*) and 1.32 eV (*C-V*). However, both measurements indicate that the barrier height slightly increases to 0.87 eV (*I-V*) and 1.44 eV (*C-V*) upon annealing at 300 °C for 1 min in nitrogen gas. After annealing at 400 °C, the Schottky barrier height slightly decreases to 0.79 eV (I-V) and 1.42 eV (C-V). Further, with an increase in annealing temperature up to 500 °C; the barrier height is decreased to 0.74 eV (*I-V*) and 1.33 eV (*C-V*). Based on the Auger electron microscopy and X-ray diffraction results, the formation of gallide phases at the Pd/n-GaN interface could be the reason for the improvement of electrical properties of Schottky contact upon annealing at 300 °C.

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1. Introduction

Gallium nitride (GaN) is a chemically stable compound semiconductor with a wide direct band gap (3.4 eV). It has potential application in the fabrication of optoelectronic devices working in the spectral range from blue to ultraviolet. GaN- related semiconductors have been used to fabricate optoelectronic devices, including visible-light emitting diodes (LEDs) [1], photo detectors [2], metal semiconductor field effect transistors (MSFETs) [3], and high electron mobility transistors (HEMTs) [4]. The characterization and the understanding of the properties of metal/GaN contacts are important because the performance of GaN-based devices can often be limited by the quality of the ohmic and Schottky contacts [5]. Hence, the development of high-quality ohmic and Schottky contacts with good thermal stability is still a challenge.

Various metals have been reported as Schottky contacts to n-type GaN by many researchers e.g., Ti [6], Au [7], Pd [8], Pt [9], Mo [10] and Ru [11]. Wang *et al.* [7] investigated the electrical characteristics of Au/n-GaN Schottky contacts with different film thicknesses. They have reported the barrier height of Au/n-GaN Schottky contacts 0.79 eV (I-V) and 1.05 eV (C-V) for a thickness of 28 nm. Weiderman *et al*. [8] investigated Pd/n-GaN Schottky diode in both *in-situ* and *ex-situ* and reported a barrier height of $0.70^{\text{in-situ}}$ and $0.90^{\text{ex-situ}}$ from I-V measurement. Suzue *et al*. [7] investigated Pt/GaN Schottky diode and reported a Schottky barrier height of 1.10 eV from I-V and C-V measurements. Ramesh *et al* [10] reported the electrical properties of Mo/n-GaN Schottky diode as a function of annealing temperature. They have shown that the barrier height of Mo/n-GaN Schottky diode were 0.81 eV (I-V) and 1.02 eV (C-V) respectively for the as deposited sample. They also shown that the Mo Schottky contact was fairly stable during annealing at 400 °C. Recently, Ramesh *et al* [11] investigated the annealing temperature effects on Ru-based Schottky contacts to n-type GaN and reported the Schottky barrier height of Ru/n-GaN and Ru/Au/n-GaN Schottky diodes with values 0.88 eV (*I-V*) and 1.10 eV (*C-V*), 0.75 eV (*I-V*) and 0.93 eV (*C-V*) respectively. In this work, we have investigated the influence of annealing effects on the electrical and structural characteristics of Pd Schottky contacts on n-type GaN (5.8×10^{17} cm^{-3}).

2. Experimental details

The n-GaN films employed in this study was grown on a *c*-plane sapphire substrate by Metal organic chemical vapor deposition (MOCVD). An undoped GaN layer thickness of 1.5 µm was grown followed by the growth of 1.5 µm thick *n*-GaN: Si ($n_d = 5.8\times10^{17}$ cm^{-3}) layer. Prior to making metal contacts, the samples were first ultrasonically degreased with warm trichloroethylene, acetone, methanol for 5 min each and then rinsed in de-ionized water. Then the degreased samples were dipped into boiling aquaregia [HNO_3: HCl = 1:3] for 10 min to remove the surface oxides and rinsed in de-ionized water. Ti (20 nm)/Al (50 nm) ohmic contacts were deposited on a portion of sample and annealed at 850 ºC in a nitrogen ambient for 1 min. Then 50 nm thick Pd (99.999 %) Schottky contact was deposited through a stainless steel mask using electron beam evaporation under a pressure of 5×10^{-6} Torr. The diameter of the Schottky dots was 1 mm. The Pd Schottky diodes were sequentially annealed at 300 ºC, 400 ºC and 500 ºC for 1 min under nitrogen ambient in rapid thermal annealing (RTA) system. The electrical characteristics of the Schottky diode were measured at room temperature by I–V and C–V using Keithley Source measuring unit (Model No. 230), and a Boonton capacitance meter (Model No. 72 B), respectively. To examine the intermixing of the metal and the GaN, Auger electron microscopy ((AES: VG: Microlab 350) depth profiling was employed. To characterize the interfacial reactions between the metal and GaN layers, X-ray diffraction (Siefert XRD PW 3710) (using Cu k_α radiation) was performed.

3. Results and discussion

The typical forward and reverse I-V characteristics of Pd/n-GaN as a function of annealing temperature are as shown in Fig 1. We fit the forward I-V characteristics using the relation for the thermionic emission over a barrier [12]

$$I = I_s \exp\left[\left(\frac{q(V-IR)}{nkT} - 1\right)\right] \quad (1)$$

$$\text{with} \quad I_S = AA^{**}T^2 \exp\left(\frac{-q\phi_b}{kT}\right) \quad (2)$$

where I_s is the saturation current, q is the electron charge, V is the applied voltage, R is the series resistance, n is the ideality factor, A^{**} is the effective Richardson constant, and ϕ_b is the Schottky barrier height. The value of ϕ_b can be deduced directly from the I–V curves if the effective Richardson constant, A^{**} is known. The theoretical value for the effective Richardson constant (26.4 A cm^{-2} K^{-2}), assumed in calculating the Schottky barrier heights, is based on the effective mass ($m^* = 0.22m_0$) of n-GaN [13]. From equation (1), a plot of ln $\{I/[1\text{-}\exp(-qV/kT)]\}$ vs V [Fig. 2 (a)] yields I_s as the intercept. Once I_s is determined, the barrier height (ϕ_b) is calculated from it. As shown in Fig. 1, it is found that all the Pd/n-GaN Schottky diodes exhibit rectifying characteristics. It is observed that the leakage current of as-deposited contact and 400 °C annealed contact are 6.86 ×10^{-8} A and 3.86 ×10^{-8} A at -1V. When the contact is annealed at relatively low temperature 300 °C, the leakage current decreased to 5.34×10^{-9} A at -1V. After annealing at 500 ºC, the leakage current is increased to 6.19×10^{-7} A at -1V. Calculations showed that the Schottky barrier height (SBH) is 0.80 eV for the as-deposited contact, 0.87 eV for 300 °C, 0.79 eV for 400 °C and 0.74 eV for 500 °C. If one assumes a negligible series resistance and that V > 3kT/q, a plot ln (I) versus V should reveal a linear region which extends over at least two decades of current. The ideality factors are 1.15±0.02, 1.04±0.02, 1.25±0.02, 1.12±0.02 for the as-deposited, 300 °C, 400 °C and 500 °C annealed contacts. The values of ideality factor are indicative of non-ideal behavior, suggesting that the transport mechanisms, other than just thermionic [14, 15, 16, 17,], are probably present in these diodes.

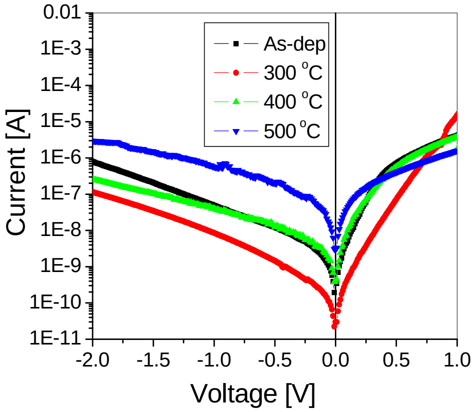

Fig. 1. The typical I-V characteristics for the Pd Schottky contact to n-type GaN as a function of annealing temperature.

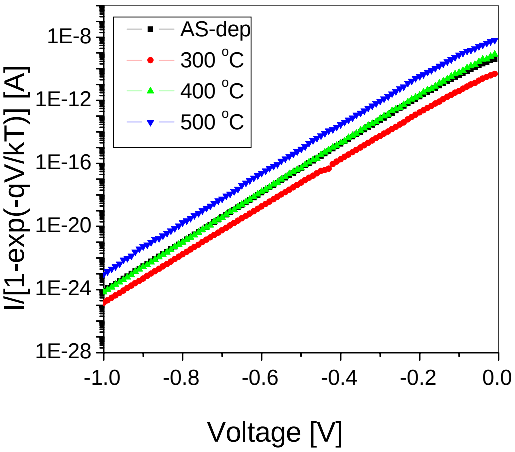

Fig. 2. Plot of I/ [1-exp (-qV/kT)] vs V for the Pd Schottky contacts annealed at different temperatures.

Capacitance voltage (C–V) characteristics of Pd/n-GaN Schottky diode were measured using a Boonton 72-B 1MHz Capacitance meter with ac test signal of 15 mV. Fig. 3 shows the plot of 1/C^2 as a function of bias voltage for as-deposited and annealed samples. The resulting plot is a straight line where the intercept with the abscissa is a measure of the barrier height while the slope is proportional to the ionized impurity concentration. The C–V relationship for Schottky diode is given by [18]

$$1/C^2 = \left(\frac{2}{\varepsilon_s qNA^2}\right)\left(V_{bi} - \frac{kT}{q} - V\right) \quad (3)$$

where ε_s is the permittivity of the semiconductor (ε_s= 9.5 ε_o), V is the applied voltage. V_o is related to the built in potential V_{bi} by the equation $V_{bi} = V_o + kT/q$, where T is the absolute temperature. The barrier height is given by the equation $\phi_b = V_o + V_n + kT/q$, where $V_n = (kT/q)\ ln\ (N_c/N_d)$. The density of states in the conduction band edge is given by $N_c = 2(2\pi m^*kT/h^2)^{3/2}$, where $m^* = 0.22m_o$ and its value is 2.53 x 10^{18} cm^{-3} for GaN [19]. The estimated Schottky barrier heights of Pd/n-GaN diode obtained by C-V are 1.32 eV for the as-deposited, 1.44 eV for 300 °C, 1.42 eV for 400 °C and 1.33 eV for 500 °C by C-V method. Table 1 shows the values of ideality factor and the Schottky barrier height for Pd/*n*-GaN Schottky diodes. It is found that the Schottky barrier height is slightly increased after annealing at 300 °C as compared with that of as-deposited contact. Further, it is observed that the Schottky barrier height is decreased with an increase in annealing temperature up to 500 °C. It can also be seen from Table 1 that the barrier heights, ϕ_b, obtained from I-V measurements are lower than those obtained from C-V measurements. This discrepancy may be due to the effects of image force on the barrier [20,21]. However, the metal probably comes into intimate contact with the semiconductor upon high temperature annealing. According to Werner and Guttler [22], spatial in homogeneities at the metal/semiconductor interface of abrupt Schottky contact can also cause such differences in the barrier height determined from I-V and C-V measurements. Another possibility may be the transport mechanism in these diodes which is not purely due to thermionic emission. For these diodes the ϕ_b obtained from I-V method is voltage or electric field sensitive, whereas the ϕ_b obtained from C-V is not.

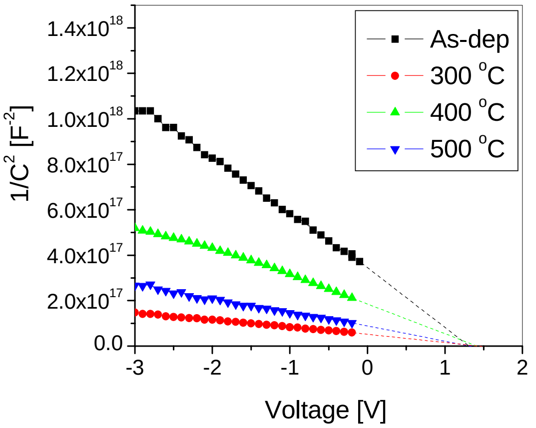

Fig. 3. Plot of $1/C^2$ vs. V for the Pd Schottky contact to n-type GaN annealed at different temperatures.

Table 1. The reverse leakage current, Schottky barrier heights and ideality factor of Pd/n-GaN Schottky diode as a function of annealing temperature.

Sample	Leakage current at -1V	Schottky barrier height (SBH), ϕ_b (eV)		Ideality factor 'n'
		I-V	C-V	
As-dep	6.86 × 10^{-8} A	0.80	1.32	1.15
300°C	5.34 × 10^{-9} A	0.87	1.44	1.04
400°C	3.86 × 10^{-8} A	0.79	1.42	1.25
500°C	6.19 × 10^{-7} A	0.74	1.33	1.12

Fig. 4 shows the AES depth profile of the Pd/n-GaN Schottky diode before and after annealing at 500 °C. As-deposited Schottky contact shows a sharp interface between Pd and GaN layers, indicating that absence of significant interdiffusion between Pd and GaN as shown in Fig. 4 (a). However, a small amount of Ga out diffused into Pd layer, indicating the possibility that Ga reacts with Pd to form gallide phases during thermal annealing temperature as shown in Fig. 4(b). For the contact annealed at 500 °C, Fig. 4(c), there is no considerable change in the interface layers as compared to that of contacts annealed at 300 °C.

Furthermore, there is no evidence that nitrogen was out-diffused into the metal layers before and after annealing at 500 °C. It is worth noting that the Pd layer remains very stable even after annealing at 500 °C.

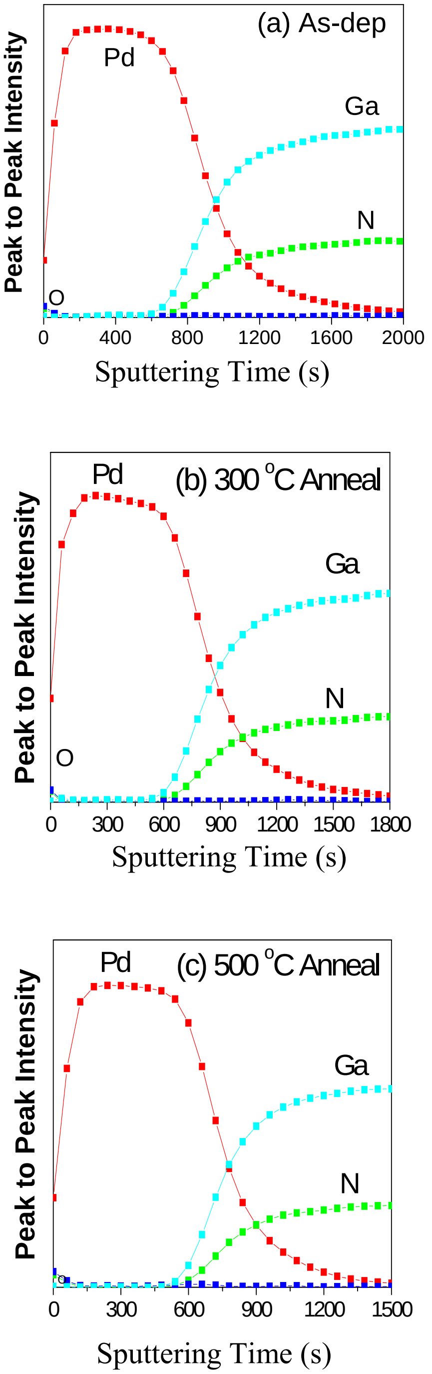

Fig. 4. Auger depth profile of the Pd Schottky contacts to n - type GaN: (a) as - deposited sample, (b) 300 °C annealed sample, and (c) 500 °C annealed sample.

Fig. 5 shows the XRD plots of the Pd/n-GaN Schottky diode before and after annealing at 500 °C. For the as-deposited sample, Fig. 5(a), in addition to the characteristic peak of GaN (002) (004) and Pd (111), there is a small peak identified as Ga_5Pd (213). Fig. 5 (b) shows the XRD plot of the sample annealed at 300 °C. In addition to the phases, which were observed in as-deposited sample, there is an additional peak, indicating the formation of new interfacial phase, as expected from AES results (Fig. 4(b)). This phase is identified as Ga_2Pd_5 (170). Further, when the sample was annealed at 500 °C, Fig. 5(c), the peak corresponding to Ga_2Pd_5 (170) found in the annealed 300 °C sample had disappeared.

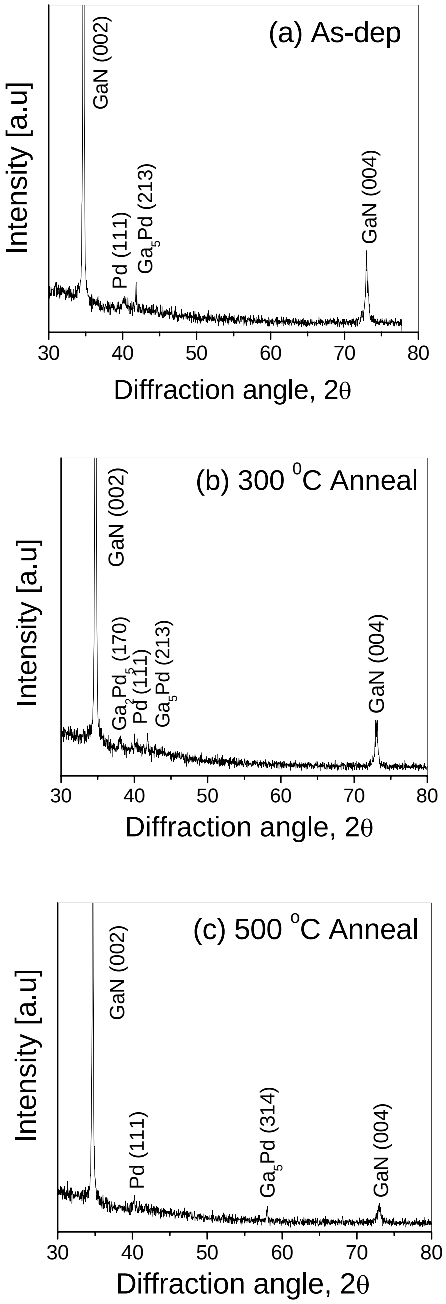

Fig. 5. XRD plot of the Pd Schottky contact to n-type GaN: (a) as-deposited sample, (b) 300 °C annealed sample, and (c) 500 °C annealed sample.

The increase in barrier height on increasing the annealing temperature could be explained as follows. The AES and XRD results evidenced the diffusion of the Pd and its reaction with GaN to form interfacial phases such as Ga_2Pd and Ga_2Pd_5 at the interface. The formation of gallide phases [as shown by the XRD results in Fig. 5 (b) and (c)] at the Pd/n-GaN interface, results in the accumulation of gallium vacancies at the GaN surface. These interfacial phases may have different work functions than the Pd contact layer, which is responsible for the increase of barrier heights. Guo et al. [23] investigated the barrier height of different Schottky metals and observed that Schottky barrier height is influenced by the interfacial product. Duboz et al. [24] observed that the nature of the metal does not play a major role in the barrier height enhancement on annealing. They have found that the Fermi level at metal/GaN interfaces is pinned by defects. Further, a modification of the defect density on annealing could change the pinning. This results in a change in the barrier height.

4. Summary

We have investigated the influence of annealing temperature on the electrical and structural properties of the Pd/n-GaN Schottky diode by current-voltage (I–V), capacitance-voltage (C-V), X-Ray diffraction (XRD) and Auger electron microscopy (AES) techniques. The barrier height of the as-deposited Schottky diode was found to be 0.80 eV (*I-V*) and 1.32 eV (*C-V*). However, the Schottky barrier height is slightly increased to 0.87 eV (*I-V*) and 1.44 eV (*C-V*) when the contact is annealed at 300 °C for 1 min in nitrogen atmosphere. After annealing at 400 °C, the Schottky barrier height is slightly decreased to 0.79 eV (*I-V)* and 1.42 eV (*C-V*). Upon increasing the annealing temperature up to 500 °C, the barrier height still decreased to 0.73 eV (*I-V*) and 1.33 eV (*C-V*). The AES and XRD results showed that the Ga_2Pd and Ga_2Pd_5 interfacial phases are formed at the metal/GaN interface upon annealing temperature at 300 °C. This may be the reason for the increase in the barrier height and a corresponding reduction of the reverse leakage current.

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