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Effect of working temperature on Ge-Nd_2O_3, Ge-Dy_2O_3, Ge-Eu_2O_3 and Ge-La_2O_3 TFTs

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TFTs having Ge as active material have been fabricated with rare earth oxides Nd_2O_3, Dy_2O_3, Eu_2O_3 and La_2O_3 as gate insulator. All the TFTs are fabricated in staggered electrode structure on perfectly cleaned glass substrates using thermal evaporation process under high vacuum. Effect of different working temperature on the TFT's characteristics has been observed and reported.

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Keywords: Ge TFTs, Rare earth oxides, Working temperature

1. Introduction

The thin film transistors (TFT) play an important role in modern electronic devices. In active matrix liquid crystal displays (AMLCDs), TFTs are used as pixel transistors [1]. The rare earth oxides Nd_2O_3, Dy_2O_3, Eu_2O_3 and La_2O_3 are found to be suitable for use as gate insulator in the TFTs due to their high thermal and chemical stability [2-4]. The various electrical parameters of the Ge-TFTs with Nd_2O_3, Dy_2O_3, Eu_2O_3 and La_2O_3 as gate insulators have been studied and these TFTs are characterized using Levinson *et.* al model [5].

Here the effect of working temperature on the TFT characteristics has been reported.

2. Experimental details

2.1 Fabrication method and the structure of the TFTs

TFTs have been fabricated in staggered electrode structure on perfectly cleaned glass substrates using thermal evaporation process by multiple pumps down (MPD) procedure. Al is deposited first as source, drain electrode over the glass substrate. Then Ge was deposited as the channel material over the source-drain electrodes. The rare earth oxide Nd_2O_3, Dy_2O_3, Eu_2O_3 and La_2O_3 were deposited as gate insulator to obtain the Ge-Nd_2O_3, Ge-Dy_2O_3, Ge-Eu_2O_3 and Ge-La_2O_3 transistors respectively. Over the oxide layer again Al is deposited to get the gate electrode. The various geometrical patterns of the films were defined by evaporation mask prepared by Al sheet. The channel length is of 50 μm which is defined by a wire grill fixed on the mask.

2.2 Measurements

The multiple beam interference method was employed to measure the thickness of the fabricated films of the TFTs. The method is capable of giving an accuracy of ±30Å [6]. The various thicknesses of the fabricated films are presented in the Table 1.

2.3 Baking of the TFTs

All the fabricated TFTs are annealed in vacuum at 250° C for about 5 hours and then stored in cleaned desiccators charged with fused $CaCl_2$ to protect the TFTs from the air contaminants.

Table 1. Thickness of the fabricated films of the TFTs

Device type	Ge-Nd_2O_3	Ge-Dy_2O_3	Ge-Eu_2O_3	Ge-La_2O_3
Thickness of the s-d electrode (Å)	1020	1070	1060	990
Thickness of the Fe film (Å)	550	580	630	500
Thickness of Nd_2O_3 Film (Å)	760	-	-	-
Thickness of the Dy_2O_3	-	810	-	-
Thickness of Eu_2O_3 Film (Å)	-	-	760	-
Thickness of La_2O_3 Film (Å)	-	-	-	850
Thickness of the gate Electrode (Å)	1000	1040	970	1030

3. Results and discussion

The variation of drain current (I_d) with respect to the different working temperatures in the forward direction (heating process) and reverse direction (cooling process) for Ge-Nd_2O_3, Ge-Dy_2O_3, Ge-Eu_2O_3 and Ge-La_2O_3 TFTs are shown in Fig. 1. In Fig. 1, the curves 'a', 'b', 'c' and'd' represent the plot of I_d vs. working temperature for Ge-Nd_2O_3, Ge-Dy_2O_3, Ge-Eu_2O_3 and Ge-La_2O_3 TFTs respectively. From the curves, it is seen that the drain current is increased slowly first upto a temperature of 100° C. Above it, the drain current increases abruptly upto a temperature of 230° C. Then the current is stabilized at a maximum value for a short range of temperature, followed by a sharp decay continues till the end of the process. The drain current (I_d) decreases continuously for the reverse direction (cooling process).

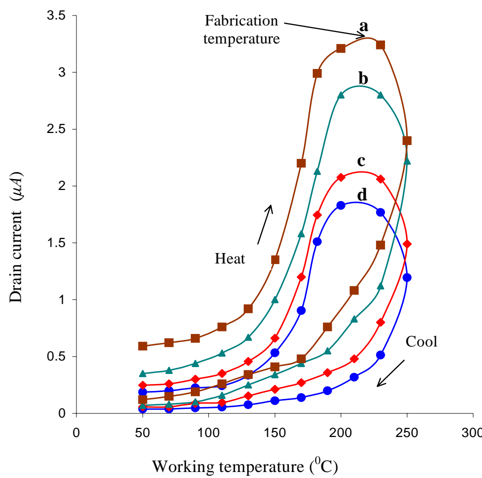

Fig. 1.Variation of drain current with working temperature (V_d = 5V, V_g= - 4V). The curves 'a', 'b', 'c' and'd' are for Ge-Nd_2O_3, Ge-Dy_2O_3, Ge-Eu_2O_3 and Ge-La_2O_3 TFTs, respectively.

The variations of drain current (I_d) with working temperature after the heating and cooling process is returned in both directions for the same TFTs (Ge-Nd_2O_3, Ge-Dy_2O_3, Ge-Eu_2O_3 and Ge-La_2O_3 TFTs) is shown in Fig. 2. In Fig. 2, the curves 'a', 'b', 'c' and'd' represent Ge-Nd_2O_3, Ge-Dy_2O_3, Ge-Eu_2O_3 and Ge-La_2O_3 TFTs respectively.

The above results that occur in case of the TFT's are due to the fact that, during the heating process (forward direction); the lattice structure of the channel is not affected at the beginning whenever it is working below the fabrication temperature (substrate temperature 250°C). Beyond the fabrication temperature, an annealing process takes place, which tend to increase the semiconductor resistivity, which lead to decrease in drain current. This change in the resistivity will remain constant. When this process is returned in both directions (heating and cooling) on the same devices, the result is observed as shown in Fig. 2 [7].

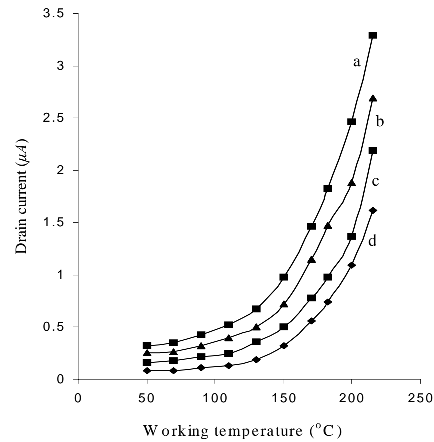

Fig. 2. Variation of drain current with working temperature after temperature stress for both directions (V_d = 5V, V_g = - 4V). The curves 'a', 'b', 'c' and'd' are for Ge-Nd_2O_3, Ge-Dy_2O_3, Ge-Eu_2O_3 and Ge-La_2O_3 TFTs, respectively

The effect of working temperature on the output characteristics of TFTs (Ge-Nd_2O_3, Ge-Dy_2O_3, Ge-Eu_2O_3 and Ge-La_2O_3) is shown in Figs. 3 and 4. In Figure 3, curves 'a_1', 'a_2', 'a_3', 'a_4' and 'b_1', 'b_2', 'b_3', 'b_4' represent the I_d vs. V_d characteristics at constant gate voltage V_g = -4V for Ge-Nd_2O_3 and Ge-Dy_2O_3 TFTs at 30° C, 90° C, 150° C and 200° C respectively. Similarly in Figure 4, curves 'c_1', 'c_2', 'c_3', 'c_4' and 'd_1', 'd_2', 'd_3', 'd_4' represent the I_d vs. V_d characteristics at constant gate voltage V_g = -4V for Ge-Eu_2O_3 and Ge-La_2O_3 TFTs at 30° C, 90° C, 150° C and 200° C respectively. From the Figs. 3 and 4, it is noted that, as the temperature increases, the drain current increases largely. This is due to the increase in kinetic energy of the charge carriers, which effectively lowers the barrier height at source-drain contacts.

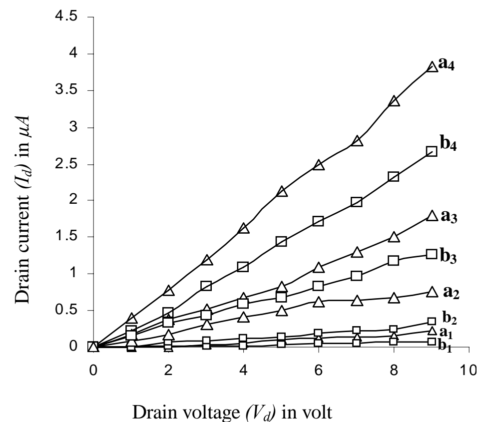

Fig. 3. Output drain characteristics of Ge- TFTs for different working temperature at V_g = - 4V. Curves 'a_1', 'a_2', 'a_3', 'a_4' represent the Ge-Nd_2O_3 TFTs at 30°C, 90° C, 150° C and 200° C respectively. Curves 'b_1', 'b_2', 'b_3', 'b_4' represent the Ge-Dy_2O_3 TFTs at 30°C, 90° C, 150° C and 200° C, respectively.

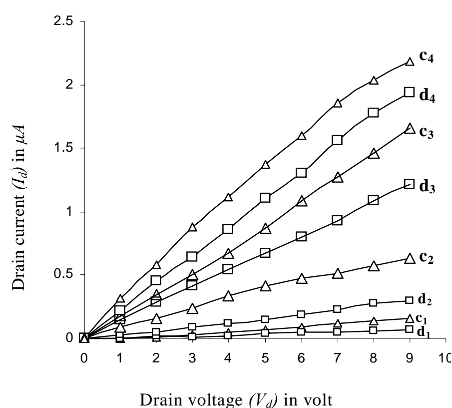

Fig. 4. Output drain characteristics of Ge- TFTs for different working temperature at V_g =- 4V. Curves 'c_1', 'c_2', 'c_3', 'c_4' represent the Ge-Eu_2O_3 TFTs at 30^oC, 90° C, 150° C and 200° C respectively. Curves 'd_1', 'd_2', 'd_3', 'd_4' represent the Ge-La_2O_3 TFTs at 30^oC, 90° C, 150° C and 200° C, respectively.

4. Conclusions

From the results observed in the case of the TFTs stated above, it may be concluded that the working temperature have adverse effect on the TFT's characteristics. Gradual increase of drain current of the TFTs occur upto the temperature 230° C. Above it the deterioration of the TFTs occurs and the drain current falls abruptly.

Acknowledgments

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