Design and simulation of half adder and half subtractor using lithium niobate-based waveguide

A. KUMARI[a], A. PAL[*,a], S. SHARMA[b,c,d]
aDepartment of Electronics & Comm. Engineering, DIT University, Dehradun-248009, India
bOMKARR Tech, New Delhi, India
ciNurture Education Solutions, Bengaluru, Karnataka, India
dDepartment of IT, Ajeenkya DY Patil University, Pune, Maharashtra, India

Half adder and half subtractor are at the core of all arithmetic operations; these optical circuits add or subtract two input bits at a time to produce sum and carry or difference and borrow as outputs, respectively. In this work, Half adder/subtractor design based on the electro-optic principle is proposed. The operating speed of the proposed design is very fast as compared to its electronic counterpart. The design consists of a Mach-Zehnder interferometer as an optical switching device. Performance parameters like extinction ratio, contrast ratio, amplitude modulation, and insertion loss have been computed and obtained as 38.34 dB, 31.87dB, 0.16 dB, and 0.025 dB, respectively for the proposed device.

1. Introduction

Electronic digital systems have limited speed and capacity to handle extensive data; to mitigate the limitation, optical technology is the right choice. Optical systems provide large bandwidth along with high data rate [1]–[5]. Optical signal processing is the new research area that offers optical computing, data processing, and ultra-fast switching [6], [7]. Researchers have proposed many next-generation optical systems to utilize the great potential of optical computation [7]. Optical waveguides are the critical element to design optical devices and circuits [8]. Till now, many optical devices like logic gates [9]–[12], code converters [13], decoders [14], [15], encoders [16], shift registers [17], [18], counters [19], flip-flop [20], [21], optical memories [22], [23], and other combinational, sequential systems have been proposed [24], [25]. Some techniques to implement various logic circuits using cross gain modulation effect in semiconductor optical amplifier (SOA) [26], cross-phase modulation in single SOA based Mach–Zehnder interferometer (MZI) [27], quantum dot semiconductor optical amplifier (QD-SOA) MZI [28], bit differential delay technique with Terahertz Optical Asymmetric Demultiplexers (TOAD) [29], nonlinear material based intensity encoded, semiconductor optical amplifier (SOA)-assisted Sagnac switch technology [30], [31], and micro-ring resonator based design [32] are good but have limitations. Cross gain and cross-phase effect in SOA is having the limitation of speed due to the saturation effect of SOA. Bit differential delay techniques are having round trip delay, which increases the time-of-flight (TOF) latency [30], [31], [33]–[36]. A half adder and subtractor

device are implemented in this work using lithium niobate-based MZI (LN-MZI). LN-MZI is a promising solution because of its characteristic features like compact size, thermal stability, integration potential, reconfigurability, and low power consumption. Optical adder and subtractor preform addition and subtraction at very high speed, used as basic building block for high-speed optical computing.

In this paper, half adder and half subtractor devices using the electro-optic effect in lithium niobate MZI have been proposed. Section 2 consists of the working principle of the MZI switch and a mathematical description. Section 3 explains the optical simulation of half adder and subtractor using MZI. Results and discussion are given in section 4. Finally, Section 5 concludes the proposed work.

## 2. Mech-Zehnder interferometer based optical switch

The Mach-Zehnder interferometer (MZI) consists of two 3 dB couplers, is designed using lithium niobate material. Lithium niobate has high electro-optic coefficient (Pockels' coefficient [37], [38]) 30.8×10^{-12} m/V and the extraordinary refractive index of 2.191. MZI is a 2x2 optical switch. A continuous-wave optical signal of 1330 nm is applied at the first input port of the MZI. The incoming signal's power is divided equally among both waveguides because the coupling coefficient is 0.5. This signal is controlled by applying an electric voltage (V) at the middle electrode of the MZI. When $V = 0$, then the optical signal is obtained at output port OUT2 and $V = 6.75\,V$ then signal appears at output port OUT1 (shown in Fig. 1 (c). Table 1 shows the optical properties of the signal used for the proposed device.
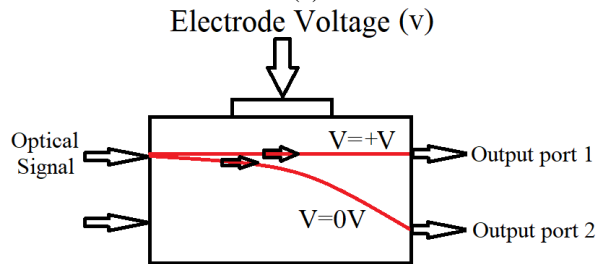
Table 1. Properties of the optical signal

Parameter	Details
Power	1 mW
Wavelength	1330 nm
Polarization	No applied
Optical Signal	Continuous-wave
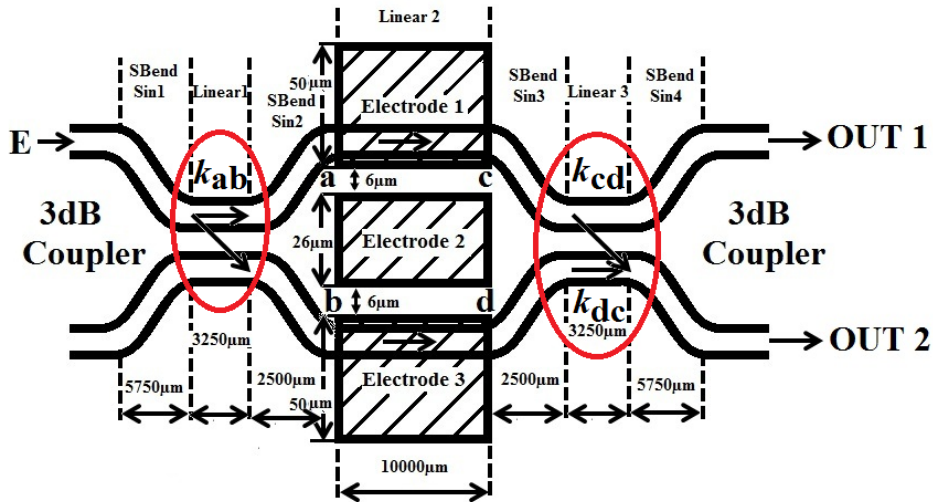
(a)
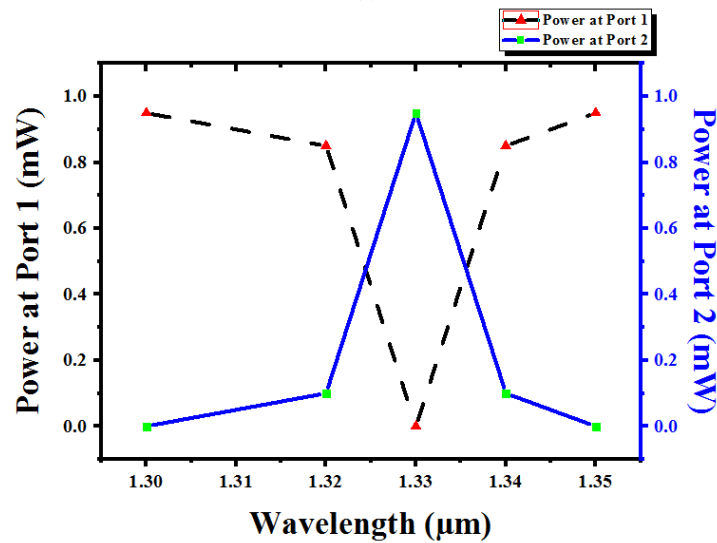
(b)

(c)

*Fig. 1. (a) Schematic view of single MZI (b) Output power at port 1 and port 2 (for zero electrode potential, V=0)
(c) Optical switching process (color online)*

Fraction k_{cd} (coupling coefficient between 3 dB coupler and output waveguide) transmit build-up signal to output port 2. The material's refractive index can be changed by applying the electric field across it (Pockel's effect). The phenomenon of changing of refractive index by an applied electric field is called the electro-optic effect; the change in the refractive index occurs. Due to this phase changes in an applied electric field. A 1 mW continuous wave is applied at input port 1. Here k_{ab} is the field coupling coefficient between the first 3 dB coupler and input waveguide, k_{cd} is coupling coefficient between the second 3 dB coupler and output waveguide. The attenuation constant is α, and insertion loss is γ. E_{in} is the input electric field applied at the first input port of the MZI. The normalized power at output port OUT1 is P_1 and at output port OUT2 is P_2. We assume that the field at point $a, b, c,$ and d are E_{ta}, E_{tb}, E_{tc} and E_{td} respectively. From Fig. 1 (a), field E_{ta}, E_{tb}, E_{tc} and E_{td} could be written as

$$E_{ta} = (1-\gamma)^{1/2}\left[\sqrt{1-k_{ab}}(E_{in}) + j\sqrt{k_{ab}}(0)\right] \quad (1)$$

$$E_{tb} = (1-\gamma)^{1/2}\left[\sqrt{1-k_{ab}}(0) + j\sqrt{k_{ab}}(E_{in})\right] \quad (2)$$

$$E_{tc} = E_{ta}e^{-j\varphi_1} \quad (3)$$

$$E_{td} = E_{tb}e^{-j\varphi_2} \quad (4)$$

The field at output ports 1 and 2 can be written as

$$OUT1 = (1-\gamma)^{1/2}\left[\sqrt{1-k_{cd}}(E_{tc}) + j\sqrt{k_{cd}}(E_{td})\right] \quad (5)$$

$$OUT2 = (1-\gamma)^{1/2}\left[j\sqrt{k_{cd}}(E_{tc}) + \sqrt{1-k_{cd}}(E_{td})\right] \quad (6)$$

After solving the above equation, and put the values of the coupling coefficient $k_{ab} = k_{cd} = 0.5$. Here insertion loss γ is assumed zero. In a simplified manner, the equations are written as:

$$OUT1 = je^{-j\varphi_0}\sin\left(\frac{\Delta\varphi}{2}\right)(E_{in}) \quad (7)$$

$$OUT2 = je^{-j\varphi_0}\cos\left(\frac{\Delta\varphi}{2}\right)(E_{in}) \quad (8)$$

where assumed that $\varphi_0 = \frac{\varphi_1+\varphi_2}{2}$ and $\Delta\varphi = \varphi_1 - \varphi_2$

Above equations 7 and 8 are helpful to design MZI as a switch.

3. Optical simulation of half adder and subtractor using MZI

Half adder is a combinational circuit having two binary bits (augend and addend) and two binary outputs (sum and carry). It adds two inputs (B add with A) and produces the sum (S) and carry (C). Half subtractor subtracts two binary inputs (B is subtracted from A) and produces difference (D) and borrow (B) as output. Table 2 has a truth table of half adder and half subtractor. Fig. 2 shows the schematic diagram of the proposed half adder and subtractor circuit. This circuit can perform addition and subtraction simultaneously. The expression for Carry (C) and Sum (S) is $C = AB$ and $S = A \oplus B$ and for difference (D) and Borrow (B) is $D = A \oplus B$ and $B = \bar{A}B$.

Here input A is applied at the second electrodes of MZI AS1, and input B is applied at MZI AS2, AS3, and AS4, respectively. There is no delay among the inputs, so no additional synchronization is required. Here an optical signal is applied at the first input port of AS1.

Table 2. The truth table of half adder and half subtractor

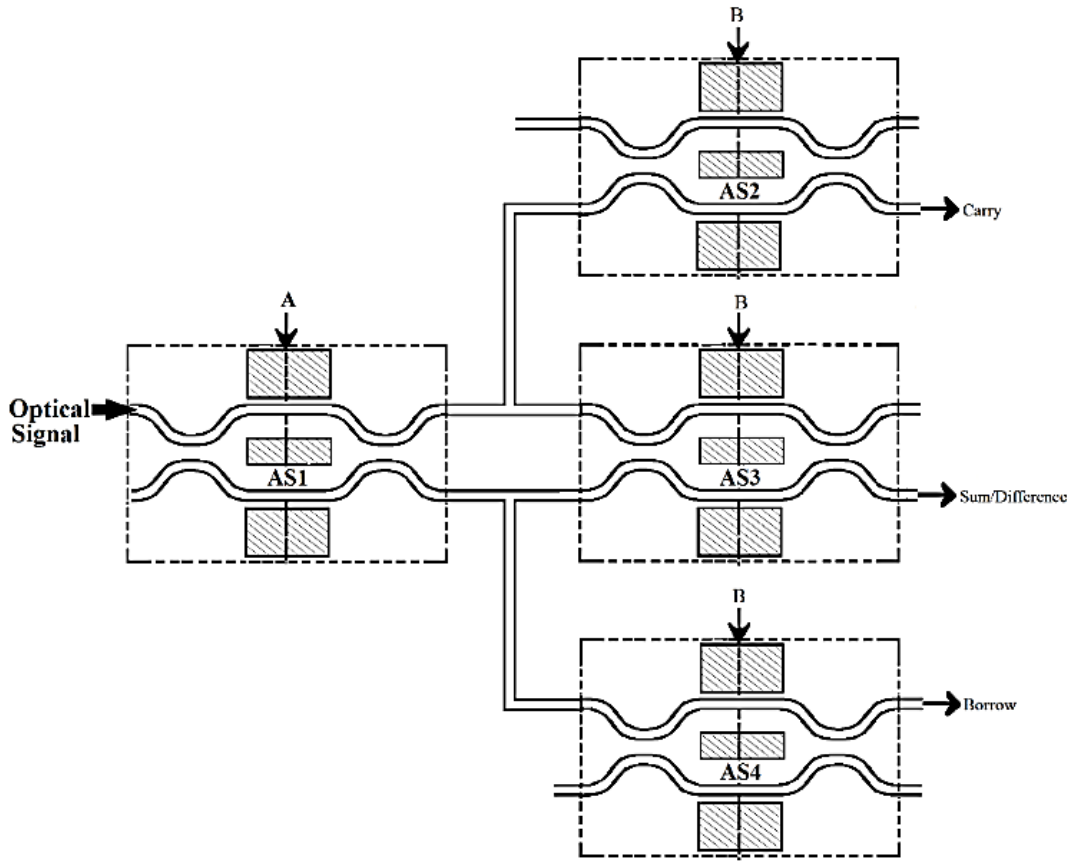| Inputs		Output of half adder/ Subtractor					
A	B	$\left(\frac{S}{D}\right)$	Power (mW)	(C)	Power (mW)	(B)	Power (mW)
Low	Low	Low	0.0886	Low	0.0604	Low	0.0675
Low	High	High	0.9994	Low	0.0023	High	0.9894
High	Low	High	0.9997	low	0.0038	Low	0.0041
High	High	Low	0.0018	High	0.9915	Low	0.0065

Fig. 2. Schematic diagram of half adder and subtractor circuit

Table 3. Simulation parameters for half adder and half subtractor

S No.	Parameters	Value(s)
1	$k_{ab} = k_{ba}$ (coupling coefficient input port)	0.50
2	$k_{cd} = k_{dc}$ (coupling coefficient output port)	0.50
3	λ operating wavelength	1.30 μm
4	Diameter of the waveguide	8 μm
5	Change of refractive index (Δn)	6×10^{-6}
6	Separation between the electrode (d)	6 μm
7	Refractive index (Electrode)	1.47
8	Electro-optic coefficient (r_{33})	30.8×10^{-12} m/V
9	Substantial length (L)	10,000 μm

The proposed structure is simulated using the beam propagation method (BPM) is shown in Fig. 3. The device has four MZIs. An optical signal is provided at the first input port of AS1. The first and second output port of AS1 is connected with the first and second output port of AS3.

The second output port of AS2 is considered as a sum/difference port. Similarly, the first and second output port of MZI AS1 is joined with the second input port of MZI AS4 and the first input port of MZI AS2. The second output of MZI AS4 shows carry (C), and the first output port of the MZI AS2 shows borrow (B).
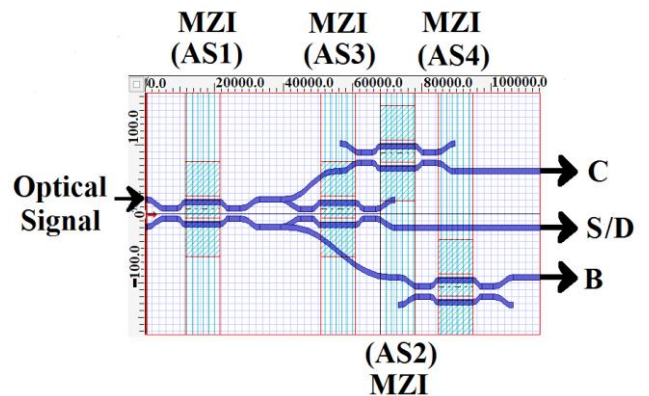

Fig. 3. BPM layout of half adder and subtractor (color online)

Various combinations of inputs A and B and corresponding outputs carry, sum/difference, and borrow for half adder, and subtractor are obtained using the beam propagation method (shown in Fig. 4). The presence and absence of light signal indicate that the signal is at logic high or a logic low.
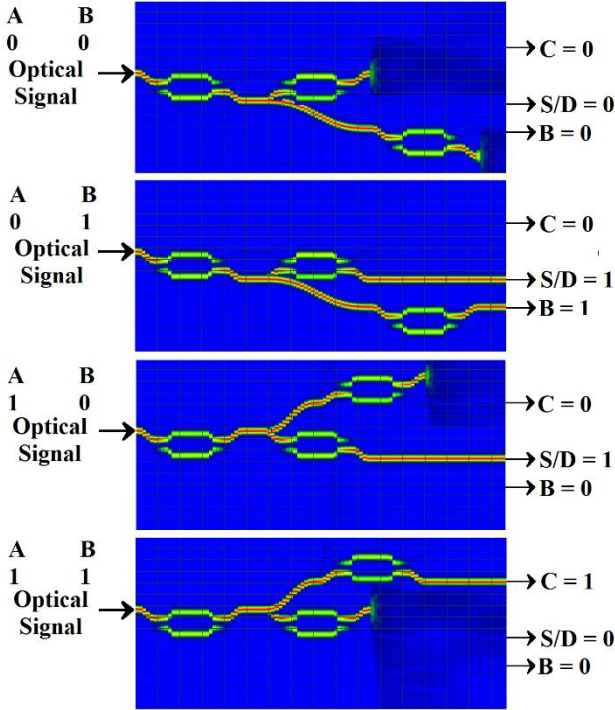

Fig. 4. Simulation result of half adder and subtractor using beam propagation method for various inputs (A, B = 00, 01, 10, 11) (color online)

The theoretical results are verified by numerical simulation. The power at output port is written as (using equations 9 and 10);

$$P_C = \left|\left|\left[e^{-j\varphi_{0AS1}} \sin\left(\frac{\Delta\varphi_{AS1}}{2}\right) e^{-j\varphi_{0AS2}} \sin\left(\frac{\Delta\varphi_{AS2}}{2}\right)\right]\right|\right| (E_{in}) \tag{9}$$

$$P_{\frac{S}{D}} = \left|\left|\left[e^{-j\varphi_{0AS1}} \sin\left(\frac{\Delta\varphi_{AS1}}{2}\right) e^{-j\varphi_{0AS3}} \cos\left(\frac{\Delta\varphi_{AS3}}{2}\right) + e^{-j\varphi_{0AS1}} \cos\left(\frac{\Delta\varphi_{AS1}}{2}\right) e^{-j\varphi_{0AS3}} \sin\left(\frac{\Delta\varphi_{AS3}}{2}\right)\right]\right|\right| (E_{in}) \tag{10}$$

$$P_B = \left|\left|\left[e^{-j\varphi_{0AS1}} \cos\left(\frac{\Delta\varphi_{AS1}}{2}\right) e^{-j\varphi_{0AS4}} \sin\left(\frac{\Delta\varphi_{AS4}}{2}\right)\right]\right|\right| (E_{in}) \tag{11}$$

where $\varphi_{1ASi} = \frac{\varphi_{1i}+\varphi_{1i}}{2}$ is the phase difference between the two arms of MZI, E_{in} is the input optical signal. Half adder and half subtractor proposed using QD-SOA requires two additional power sources to pump optical

signals from one port to another. Implementing a simple circuit using QD-SOA requires more components; the complexity of the circuit is increased. In addition, an injection current is also required. In lithium niobate-based MZI, no injection is needed, and able to operate at 160Gbps. Unlike QD-SOA, different wavelength signals and orthogonally polarized light signals are not required.

4. Results and discussion

The performance parameter of the proposed half adder and subtractor device, extinction ratio (ER), contrast ratio (CR), amplitude modulation (AM), insertion loss (IL), and relative eye-opening (Eye), has been computed from the simulated output [39], [40].

$$\text{ER (dB)} = 10\log\left(\frac{P_{min}^1}{P_{max}^0}\right) \tag{12}$$

$$\text{CR (dB)} = 10\log\left(\frac{P_{mean}^1}{P_{mean}^0}\right) \tag{13}$$

$$\text{AM (dB)} = 10\log\left(\frac{P_{max}^1}{P_{min}^0}\right) \tag{14}$$

$$\text{IL (dB)} = 10\log\left(\frac{P_{out}}{P_{in}}\right) \tag{15}$$

$$\text{Eye} = \left(\frac{P_{min}^1 - P_{max}^0}{P_{min}^1}\right) \times 100\% \tag{16}$$

where P_{max}^1 (P_{max}^0), P_{mean}^1 (P_{mean}^0) and P_{min}^1 (P_{min}^0) are the maximum, mean, and minimum values of power at the output for high '1' (low '0') levels. P_{out} and P_{in} are the power at the output and input port, respectively.

The high value of ER is desirable for switching the optical signal. Fig. 5 is a plot between extinction ratio vs. wavelength, and Fig. 6 depicts the relation between ER and coupling ratio. Max extinction ratio (38.34dB) is achieved at 1.3 µm. The coupling ratio is taken 0.5 for the device, and maximum ER is obtained at this point.

For proper operation of the device, the contrast ratio should be high as possible so that maximum input power is delivered at the output port. The value of the CR is calculated, and its value found 31.87 dB, 28.19 dB, and 30.29 dB (Fig. 7) for carry, sum/difference, and borrow, respectively. The amplitude modulation should be small. Fig. 8 shows a variation of amplitude modulation vs. wavelength.
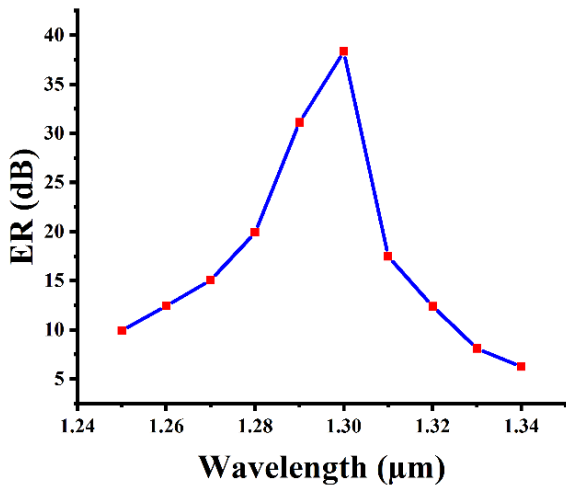
Fig. 5. Extinction ratio vs. wavelength (color online)
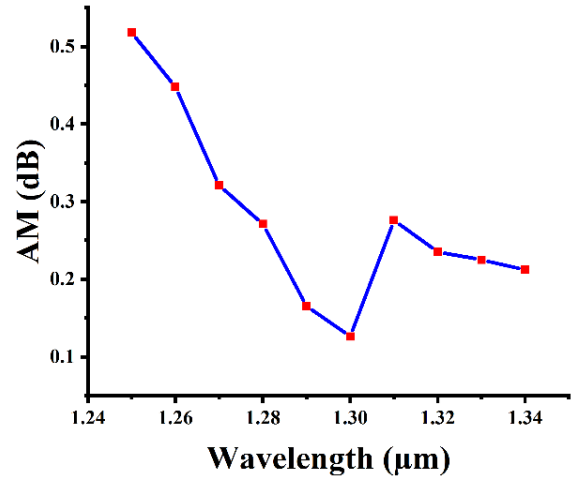

Fig. 8. Amplitude modulation vs. wavelength (color online)
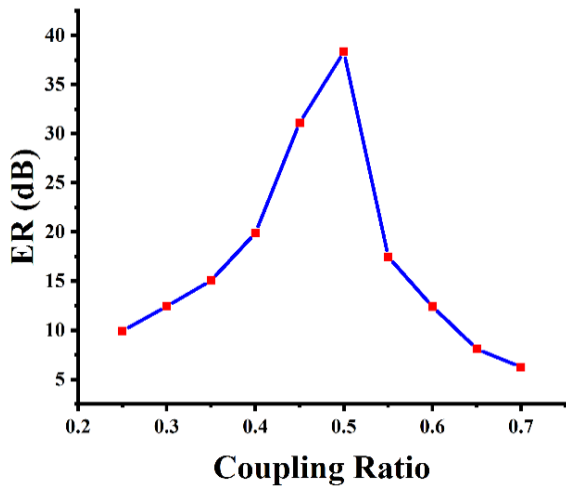

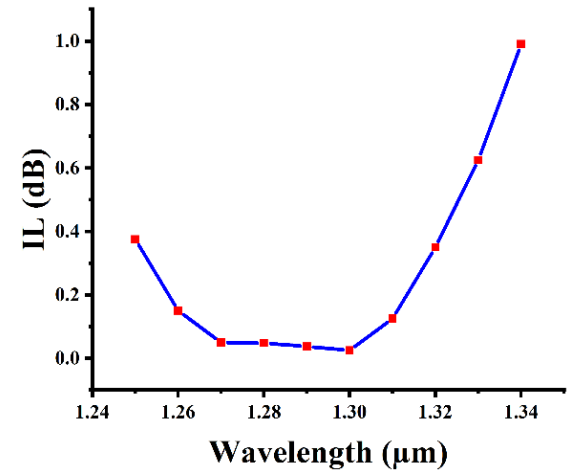Fig. 6. Extinction ratio vs. coupling ratio (color online)

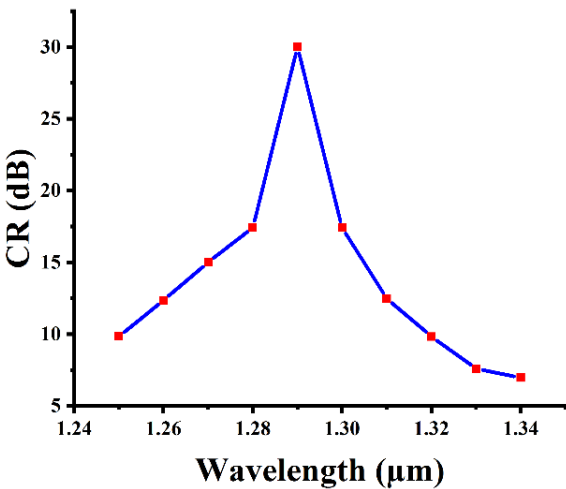Fig. 9. Insertion loss vs. wavelength (color online)

Fig. 7. Contrast ratio vs. wavelength (color online)

Table 4. Compared parameters values with the others work

Parameter	Carry (C)	(S/D)	Borrow (B)	Ref
Extinction ratio (ER)	16.91 dB	8.77 dB	-	
Contrast ratio (CR)	19.73 dB	11.82 dB	-	
Amplitude modulation (AM)	0.09 dB	0.09 dB	-	[41]
Insertion loss (IL)	-	-	-	
Eye opening	97.0%	86.7%	-	
Extinction ratio (ER)	38.34 dB	35.89 dB	37.04 dB	
Contrast ratio (CR)	31.87 dB	28.19 dB	30.29 dB	
Amplitude modulation (AM)	0.16 dB	0.20 dB	0.18 dB	Proposed
Insertion loss (IL)	0.025 dB	0.098 dB	0.081 dB	
Eye opening	94.7%	85%	93.1%	

Table 4 consists of the analysis of the comparative parameter of the proposed device. Fig. 10 consists of an eye diagram for the sum/difference of the half adder and subtractor device. The eye-opening for the device is desirable, and it is obtained 85% for the sum/difference output port (from Table 4).

Simulation results of half adder and half subtractor are verified successfully using MATLAB, as shown in Fig. 11, which indicates the proper operation of the device.
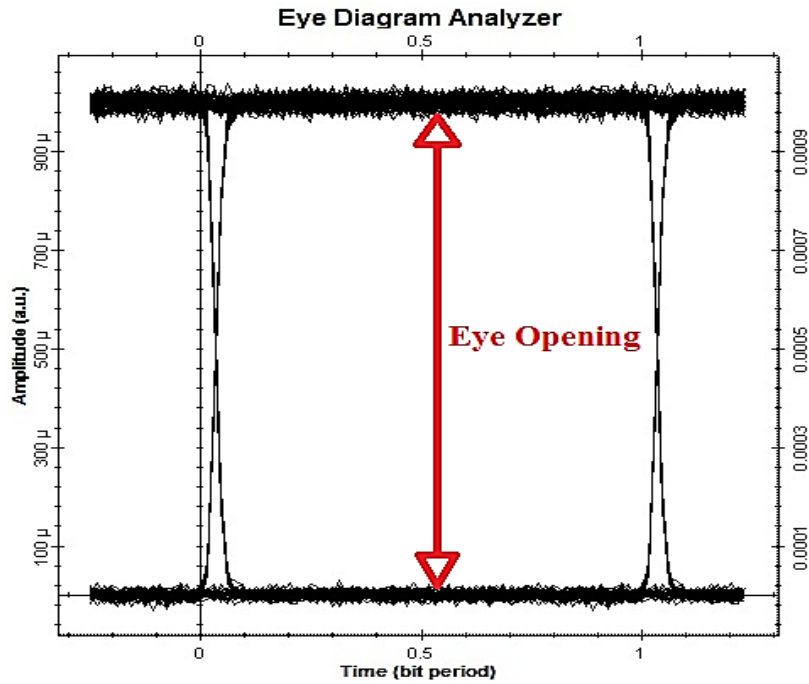

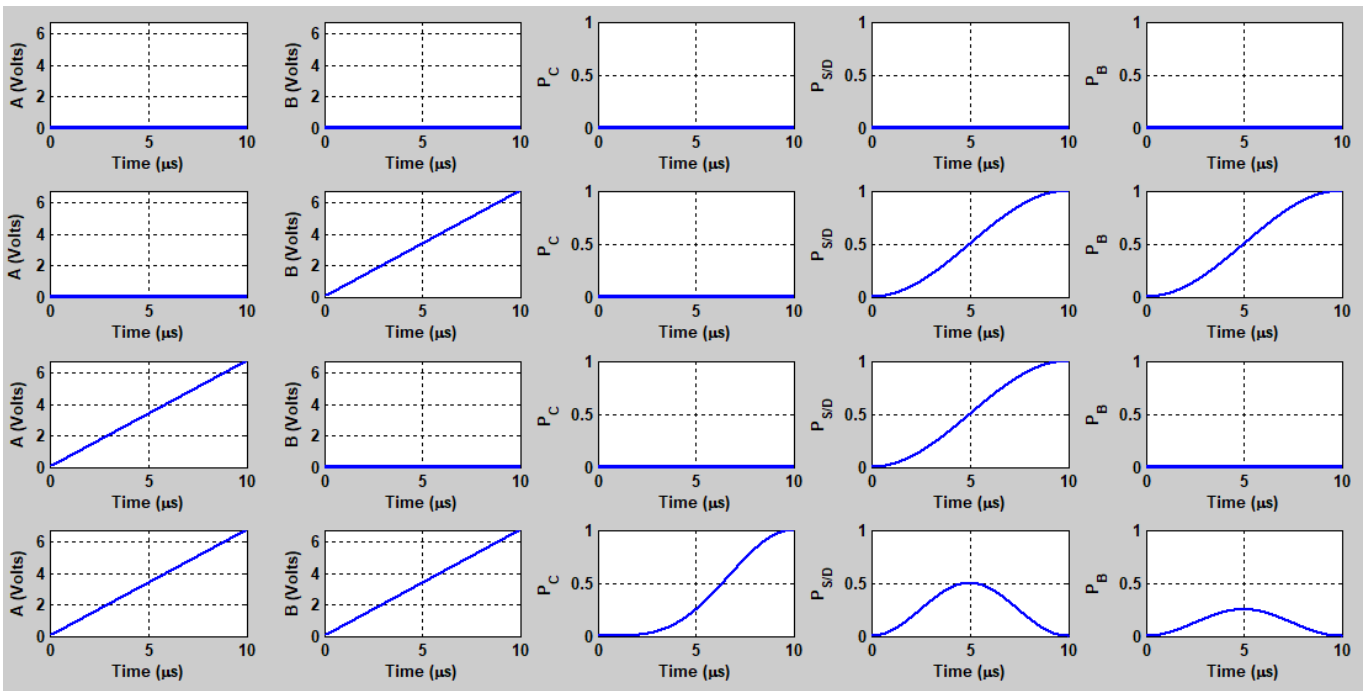Fig. 10. Eye diagram for the sum/difference of half adder and subtractor

Fig. 11. MATLAB results for half adder and subtractor

Half adder and half subtractor are the basic arithmetic unit in the digital system. A full adder circuit can be implemented using two half adders, able to add three bits and produce the sum and carry as output. In this work, the optical cost of the circuit is computed based on the number of MZI elements are used, and delay (Δ) is estimated as

the number of cascaded structures of MZI elements by unit delay (Δ). Here no other components like beam combiner and beam splitter are used, which are necessary for the SOA-based devices.
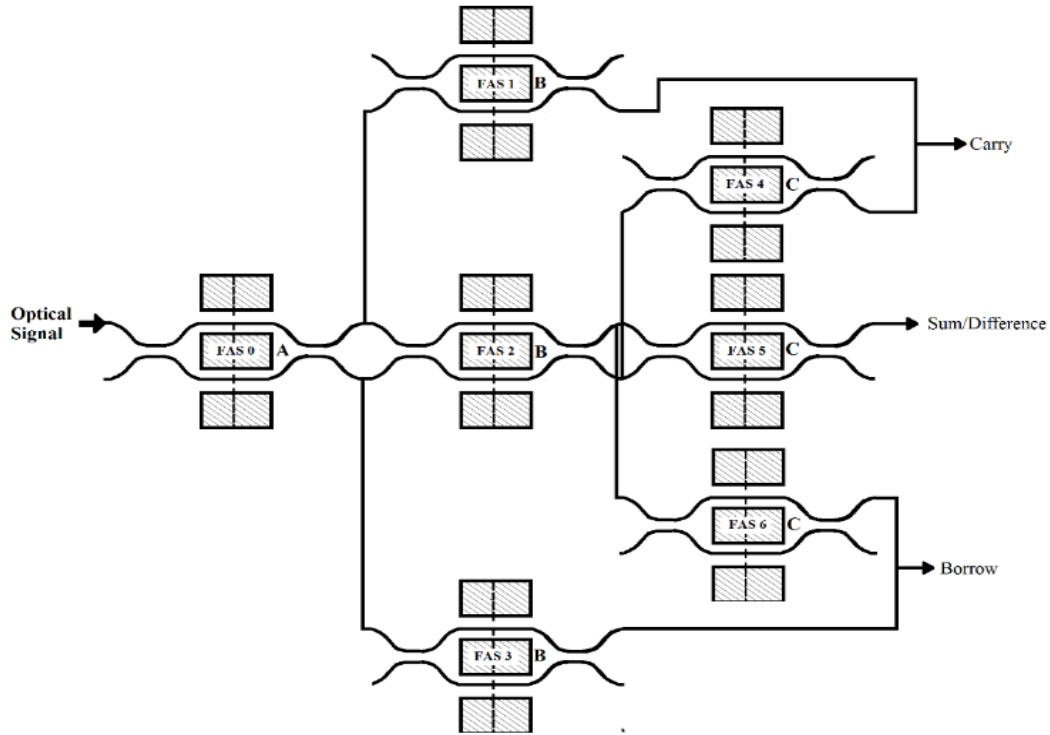

Fig. 12. Full adder and full subtractor

Table 5. Cost estimation for the proposed adder and subtractor circuit

Device	No. of MZI	Optical cost	Operational delay
Half adder	3	3	2Δ
Full adder	5	5	3Δ
Half subtractor	3	3	2Δ
Full subtractor	5	5	3Δ
Parallel adder	$5n$	$5n$	$3n\Delta$
Adder and subtractor	$7n$	$7n$	$3n\Delta$

After a discussion of the full adder and subtractor, a parallel adder and subtractor circuit is proposed. Here two-bit adders and subtractors are described (Shown in Fig. 13). Control signal M is the mode selector. If $M = 0$, then it will work as an adder circuit, and if $M = 1$, then it will work as a subtractor. O-E is optical to electrical signal conversion, consists of a photodiode and amplifier. Here subtraction is performed using 2's complement method.
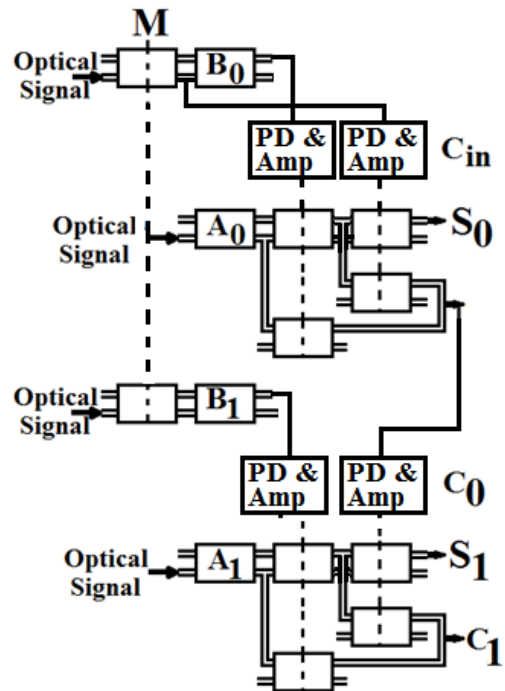

Fig. 13. Binary parallel adder subtractor circuit

In Fig. 14, the four-bit binary parallel adder circuit is proposed. The cost estimation for the parallel adder and parallel adder subtractor circuit is given in Table 5. The comparative optical cost estimation reported by others is given in Table 6.
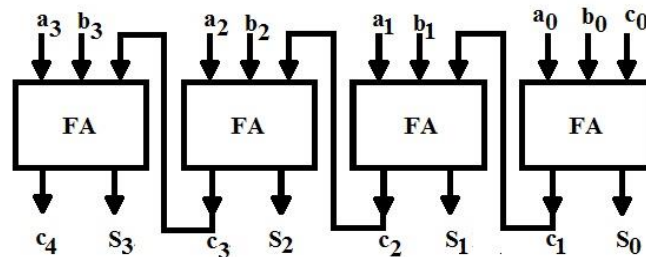

Fig. 14. Binary parallel adder circuit

Table 6. Optical cost and delay assessment with other reported work

Ref	Thomsen et al. [42]	Nair et al. [43]	Thapliyal et al. [44]	Kotiyal et al. [45]	Datta et al. [41]	Proposed work				
						HA	FA	HS	FS	PA
Optical cost	$8n - 8$	$18n - 8$	$19n + 5$	$6n + 2$	$4n$	3	5	3	5	$5n$
Delay (Δ)	$3n + 2$	$4n + 1$	$4n + 4$	$3n + 1$	$2n$	2	3	2	3	$3n$

5. Conclusion

In this paper, the half adder and subtractor, with the help of Mach–Zehnder interferometers-based switch, is realized. Both these circuits are realized using a single circuit. These circuits are elementary for the arithmetic of binary data manipulations and have various applications in optical computing. This paper explains the successful design of the circuit mentioned above using the electro-optic effect of LiNbO3 MZI in BPM and mathematical description. These results are verified using MATLAB simulations. For the proposed device extinction ratio, 38.34 dB has been obtained and much better than the permissible limits.

References

[1] M. Galili et al., Photonics **1**(2), 83 (2014).
[2] M. Shioda, I. Yokota, Y. Sugaya, S. Saito, H. Ogiwara, Fujitsu Sci. Tech. J. **49**(3), 342 (2013).
[3] T. Kaur, G. Soni, International Journal of Computer Science and Mobile Computing **4**(10), 40 (2015).
[4] K. Vlachos, N. Pleros, C. Bintjas, G. Theophilopoulos, H. Avramopoulos, Journal of Lightwave Technology **21**(9), 1857 (2003).
[5] L. Huo, D. Wang, Q. Wang, Y. Xing, X. Jiang, C. Lou, Photonic Netw. Commun. **32**(2), 197 (2016).
[6] K. Singh, G. Kaur, M. L. Singh, Opt. Eng. **55**(7), 077104 (2016).
[7] S. C. Xavier, K. Arunachalam E. Caroline, W. Johnson, Opt. Eng. **52**(2), 025201 (2013).
[8] Y. Xie, Z. Zhang, T. Song, C. He, J. Li, G. Wang, Opt. Eng. **55**(5), 056110 (2016).
[9] F. K. Law, M. R. Uddin, H. Hashim, Z. Hamid, Opt. Quantum Electron. **49**(413), 1 (2017).
[10] M. A. Jasim, A. Aldalbahi Electronics **8**(2), (215), 1 (2019).
[11] H. Yang et al., Sci. Adv. **4**(7), 1 (2018).
[12] A. Pashamehr, M. Zavvari, H. Alipour-Banaei, Front. Optoelectron. **9**(4), 578 (2016).
[13] A. Pal, S. Kumar, S. Sharma, J. Opt. Commun. **38**(2), 117 (2017).
[14] A. Pal, S. Kumar, S. Sharma, Photonic Netw. Commun. **35**(1), 79 (2017).
[15] S. Kaur, Optik **124**(17), 2650 (2013).
[16] A. Pal, S. Kumar, S. Sharma, S. K. Raghuwanshi, Optical Modelling and Design IV **9889**, 98890H (2016).
[17] H. Zoweil, Egypt. J. Basic Appl. Sci. **3**(3), 322 (2016).
[18] S. Kaur, R. S. Kaler, Opt. Quantum Electron. **46**(8), 991 (2013).
[19] S. Kaur, R. S. Kaler, J. Opt. **16**(3), 035201 (2014).
[20] S. Mandal, Opt. Eng. **56**(6), 066105 (2017).
[21] A. Pal, S. Kumar, S. Sharma, J. Opt. Commun. **40**(2), 119 (2017).
[22] Y. Ben Ezra, B. I. Lembrikov, 18th International Conference on Transparent Optical Networks (ICTON), 5 (2016).
[23] C. Vagionas, P. Maniotis, S. Pitris, A. Miliou, N. Pleros, Appl. Sci. **7**(7), 1 (2017).
[24] S. Abdulnabi, M. Abbas, Photonics **6**(1), 30 (2019).
[25] L. Wang, Y. Wang, C. Wu, F. Wang, Photonics Sensors **6**(4), 366 (2016).
[26] K. E. Zoiros, P. Morel, AIP Advances **4**(7), 077107

(2014).

[27] M. S. Ab-Rahman, A. A. Swedan, Open Phys. **15**(1), 1077 (2017).

[28] A. Kotb, K. E. Zoiros, C. Guo, J. Comput. Electron. **18**(2), 628 (2019).

[29] S. Soysouvanh, P. Phongsanam, S. Mitatha, J. Ali, P. Yupapin, I. S. Amiri, K. T. V Grattan, M. Yoshida, Microsyst. Technol. **25**(2), 431 (2018).

[30] T. Chattopadhyay, Optik **123**(21), 1961 (2012).

[31] K. Kaur, K. S. Bhatia, J. Opt. Commun. **36**(4), 297 (2015).

[32] J. K. Rakshit, J. N. Roy, Opt. Appl. **XLVI**(4), 517 (2016).

[33] N. K. Srivastava, S. K. Raghuwanshi, Optik **156**, 571 (2018).

[34] Y. Singh, S. K. Raghuwanshi, M. Kumar, Proceedings Volume 10539, Photonic Instrumentation Engineering V; 105391A (2018) SPIE OPTO, 2018, San Francisco, California, United States.

[35] Y. Singh, S. K. Raghuwanshi, Proceedings Volume 10925, Photonic Instrumentation Engineering VI; 1092516 (2019) SPIE OPTO, 2019, San Francisco, California, United States.

[36] Y. Singh, S. K. Raghuwanshi, Optik **181**, 748 (2019).

[37] H. Jiang, Y. Chen, G. Li, C. Zhu, X. Chen, Opt. Express **23**(8), 211 (2015).

[38] A. Kumar, S. Kumar, S. K. Raghuwanshi, Opt. Commun. **324**, 93 (2014).

[39] K. E. Zoiros, A. Kalaitzi, C. S. Koukourlis, Optik **121**(13), 1180 (2010).

[40] D. K. Gayen, T. Chattopadhyay, R. K. Pal, J. N. Roy, Chinese Opt. Lett. **9**(6), 6 (2011).

[41] K. Datta, T. Chattopadhyay, I. Sengupta, Microelectronics J. **46**(9), 839 (2015).

[42] M. K. Thomsen, R. Glück, H. B. Axelsen, J. Phys. A Math. Theor. **43**(38), 382002 (2010).

[43] Nivedita Nair, Sanmukh Kaur, Hardeep Singh, Optik **231**, 166325 (2021).

[44] H. Thapliyal, N. Ranganathan, Design, Automation & Test in Europe **2011**, 1-4 (2011), DOI: 10.1109/DATE.2011.5763308.

[45] S. Kotiyal, H. Thapliyal, N. Ranganathan, Design, Automation & Test in Europe Conference & Exhibition **2012**, 721 (2012).

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*Corresponding author: amrindra.ieee@gmail.com

Appendix A1

The detailed simulation process for the proposed design is given below:

Case 1: $A = 0, B = 0$

An optical signal is applied at the first input port of the MZI AS1. The control signal $A = 0$, so the optical signal is obtained at the second output port of the MZI AS1. This port is connected with the second input port of MZI AS3 and the first input port of MZI AS4. Since control signal $B = 0$, the output signal is obtained at the first output port of MZI AS3 and the second output port of the MZI AS4, i.e., $S/D = 0, B = 0$. The optical power at the first output port of the MZI AS1 is zero, so no signal emerges at the second output port of the MZI AS2, i.e., $C = 0$. So the output of the adder is $S/D = 0, C = 0$ and the result of the subtractor is $S/D = 0, B = 0$.

Case 2: $A = 0, B = 1$

As discussed in the previous case, if $A = 0$, then an optical signal is obtained at the second output port of the MZI AS1. No power emerged at the second input port of the MZI AS2, so control signal $B = 1$ does not make any change at the second output port of the MZI AS2, so $C = 0$. Control signal $B = 1$, the incoming optical has emerged at the second output port of MZI AS3, and first output port of the MZI AS4, i.e., $S/D = 1, B = 1$ output of the half subtractor is verified. The output of the half adder is $S/D = 1, C = 0$.

Case 3: $A = 1, B = 0$

The control signal $A = 1$, an optical signal is obtained at the first output port of the MZI AS1. The control signal $B = 0$, the incoming optical signal is obtained at the first output port of the MZI AS2 (i.e., $C = 0$) and the second output port of the MZI AS3 ($S/D = 1$). The output of the adder will be $S/D = 1, C = 0$. The input of the MZI AS4 is zero, so output at the first output port of the will be zero, i.e., $B = 0$. The result of the subtractor is $S/D = 1, B = 0$.

Case 4: $A = 1, B = 1$

As discussed in the previous case, $A = 1$, an optical signal emerges at the first output port of the MZI AS1. This output port is connected with the second input port of MZI AS2 and the first input port of MZI AS3. Since the control signal $B = 1$, the optical signal is obtained at the second output port MZI AS2 and the first output port of the MZI AS3, i.e., $S/D = 0, C = 1$. The output of the adder circuit is $S/D = 0, C = 1$. The input of the MZI AS4 is zero, so the result at the first output port of the will be zero, i.e., $B = 0$. The result of the subtractor is $S/D = 0, B = 0$.

Above all, the cases are varied with the truth table Table 2 of the half adder and subtractor.

Appendix A2

Fig. 13 is the extension of the half adder and subtractor circuit. Fig. 13 is a 2-bit parallel adder and subtractor circuit. The two-bit numbers are A_1A_0 and B_1B_0. When we add parallel

$$C_0$$
$$A_1 A_0$$
$$B_1 B_0$$
$$\overline{}$$
$$C_1 S_1 S_0$$

The result will be $C_1 S_1 S_0$.

Table A1. A truth table for parallel adder and subtractor circuit

M	A_1	A_0	B_1	B_0	C_1	S_1	S_0
Adder							
0	0	0	0	1	0	0	1
0	1	1	1	1	1	1	0
Subtractor							
0	0	0	0	1	0	1	1
0	1	1	1	1	1	0	0

Fig. A2.1 shows the binary parallel adder and subtractor circuit with addition operation, and Fig. A2.2 shows the binary parallel adder and subtractor with subtraction operation. Two cases are verified using the beam propagation method and given for your reference. Similar other cases can be realized. Table A1 consists of the truth table for the binary parallel adder and subtractor circuit.
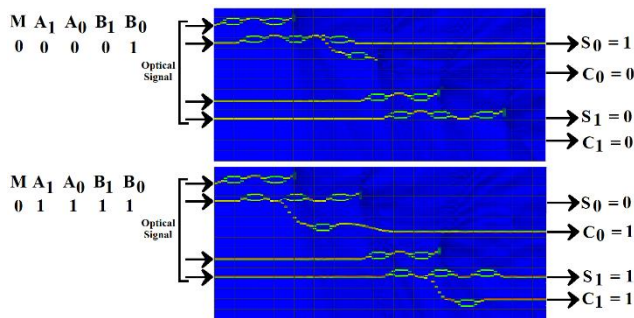

Fig. A2.1: Binary parallel adder and subtractor (addition operation) (color online)
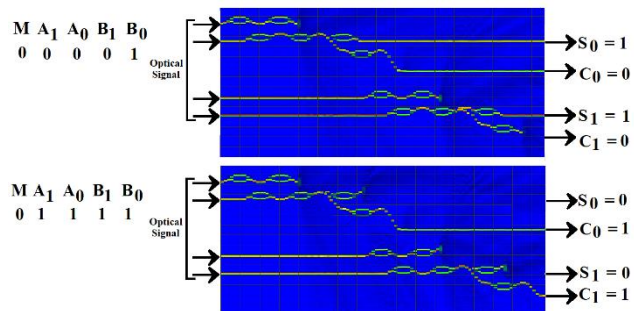

Fig. A2.2: Binary parallel adder and subtractor (subtraction operation) (color online)

In Fig. A2.3, the two-bit binary parallel circuit is designed. Two cases are simulated using BPM. Similarly, cases can be realized using the proposed design. Further, a four-bit parallel adder circuit can be implemented. Table A2 shows the truth table for the parallel adder circuit.

Table A2: Truth table for parallel adder

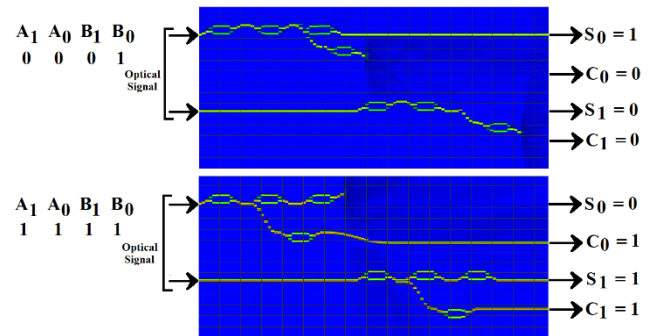| A_1	A_0	B_1	B_0	C_1	S_1	S_0
0	0	0	1	0	0	1
1	1	1	1	1	1	0

Fig. A2.3: 2 Bit parallel adder (color online)