Design and performance analysis of pentacene organic field effect transistor with high-Kdielectric materials

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This research work presents various macroscopic parameters, molecular and microscopic characteristics of organic field effect transistor (OFET). The parameters influence charge transport processes in OFET models, field effect mobility, disorder, trap existence, threshold voltage and current on/off ratio. The current study investigates into top contact organic field effect transistors (OFETs) with uniform and unequal mobility zones using two-dimensional finite element-based device models. Several calibrated simulation standards are created to imitate the morphological disorder in structure, such as taking variable low mobility zones surrounding contacts into consideration. The effect of variation of the channel length from 20µm to 50µm and dielectrics changes in drain current, threshold voltage, current on/off ratio are studied. Furthermore, the dielectric layer of an OFET is changed with SiO_2, Al_2O_3, and HfO_2 dielectric materials without affecting the dielectric thickness, which improves device dependability. The device's performance is improved with high-k dielectric material. The electrical parameters extracted for HfO_2 OFET at 20µm channel length are I_{on} = -7.38 x 10^{-7}, I_{off} = -3.19 x 10^{-14}, I_{on}/I_{off} = 2 x 10^{7}, V_{TH} = -0.75, SS=0.0705 and high drain current value of -1.63 x 10^{-5} A at gate and drain voltage of 3.0V where it showed an improvement of 28.23% in drain current along with 51.88% improvement in current on/off ratio. Due to these improved features, we can utilize OFET in various switching and sensing applications.

(Received December 13, 2022; accepted August 7, 2023)

Keywords: OFET, Pentacene, Organic Semiconductor (OS), Bottom Gate Top Contact (BGTC), MOSFET, Subthreshold Slope, High-K dielectric

1. Introduction

Organic field effect transistors (OFET) applications research has accelerated dramatically in the last 30 years. OFETs promise in low-cost, flexible, lightweight, low fabrication temperature and environmentally friendly semiconductor devices. It has wide applications such as active-matrix backplanes in displays, biosensors, gas sensors and radio frequency identification tags (RFIDs) [1]–[7], despite their lower electron mobility than typical semiconductors. Inorganic semiconductors, on the other hand, have limited stretching capabilities, so cannot be manufactured on plastic or any other flexible substrate. They also need extra manufacturing stages and a dust-free environment, resulting in a higher fabrication cost. The electrical and chemical characteristics, as well as the electronic structure of these devices, need be properly defined and understood in order to efficiently construct organic devices that can compete at the same level as inorganic semiconductor devices. The commercial benefit of OFETs for next-generation devices is that they may be processed in a variety of methods, such as solution casting, ink-jet printing, spin coating, and so on. Because OFETs have less leakage current, a lower processing temperature, and need fewer fabrication steps than MOSFETs [10], OFETs are a viable option for bulk-Si transistors in terms of good performance and low fabrication cost.

The performance of an OFET is heavily influenced by the gate oxide layer, insulator and organic contact quality, organic film structure, and charge injection process [8]–[12]. To reduce leakage current, it is critical to design devices with low operating voltage and less power consumption and this feature can be used in applications such as flat panels, transistor-driven flexible OLEDs, and portable electronics [13]. The use of different contact materials, self-assembled monolayer treatment, and injection layers that improve capacitance by lowering interfacial trap densities and charge dispersion are some of the methods for achieving low turn on voltage. Device modelling for circuit simulation is frequently performed using a device model that is utilized to simulate the physical processes in the device utilizing various semiconductor equations [14]. Recently, we've observed Pentacene OTFTs make considerable advances in device performance of OFETs, which are now equivalent to amorphous hydrogenated silicon TFTs [15]. However, as compared to inorganic transistors, this performance is insufficient [29]. There is still more effort to be done to improve the electrical properties, uniformity and dependability. Experiments to enhance OFET efficiency by varying the conductivity, semi conductivity, and insulating characteristics of different layers on a substrate. The surface roughness, the density of surface traps, and the dielectric constant are all important characteristics. Most OFETs are using an insulator made of an oxide

(mostly silicon oxide SiO_2) [30]-[33]. This type of OFET requires a relatively high voltage for operation, but the low dielectric constant remains a serious limitation for low power because operating voltages largely above 10 V are required for sufficient charge injection in the channel. High-K materials such as Al_2O_3 and HfO_2 have been used as gate dielectrics in OFETs to allow them to operate at low voltages and hence reduce power consumption.

2. Device structure and numerical simulation

Device geometry is critical to the characterization of OFETs because it enlightens one about carrying Semiconductor, the dielectric, and three electrodes, namely drain, source, and gate, are all arranged on the substrate in OFETs as shown in Fig. 1. The position of three electrodes with regard to the semiconductor layer, architecture is divided into four types: (1) Bottom Gate Bottom Contact (BGBC) (2) Bottom Gate Top Contact (BGTC) (3) Top Gate Bottom Contact (TGBC) (4) Top Gate Top Contact (TGTC) as depicted in Fig. 2. The S/D electrodes are separated from the semiconductor–dielectric interface in a top contact configuration, which means charge carriers must travel over the Organic Semiconductor (OS) layer to reach the channel.

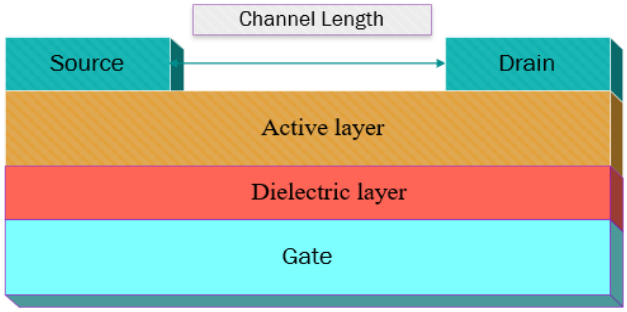

Fig. 1. OFET structure (color online)

Top contact is a configuration in which the S/D electrodes are located distant from the semiconductor–dielectric interface, which forces charge carriers to travel over the OS layer to reach the channel. Bottom contact is a different design in which the S/D electrodes connect to the channel at the semiconductor–dielectric interface, where the bulk of the charge carriers are predicted to travel. The advantage of a top contact is that it has a longer channel length and lower contact resistance because the gate electrode, insulator and S/D connections are all pre-fabricated where the semiconductor is deposited in the final step of the process. The BGBC structure provides for rapid testing of new semiconductor materials and processing methods.

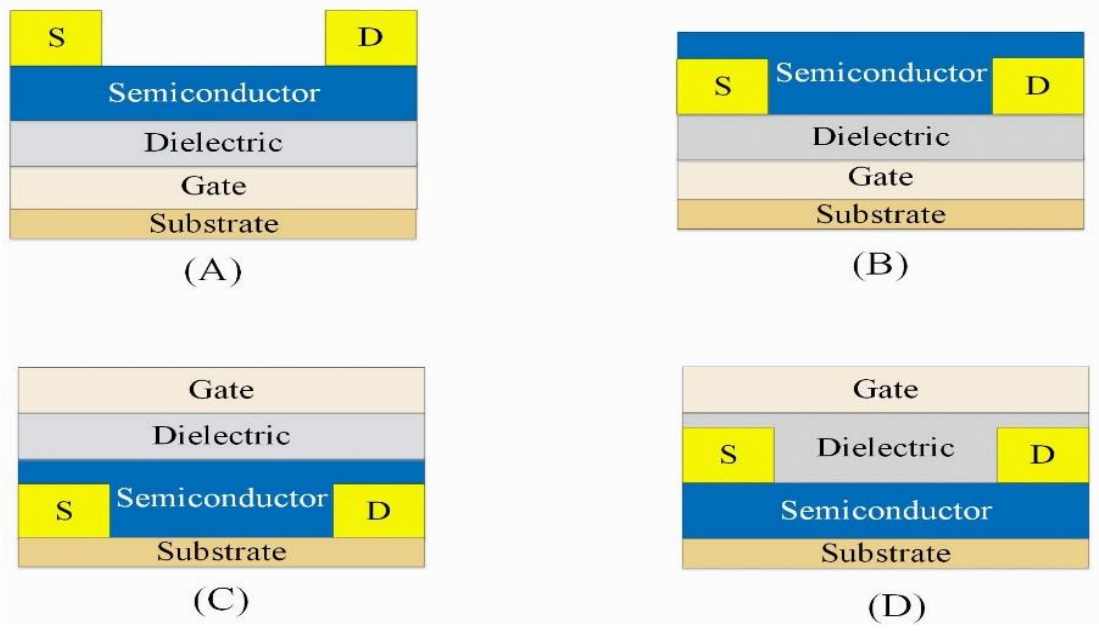

Fig. 2. Different OFET configurations (A) BGTC (B) BGBC (C) TGBC (D) TGTC(color online)

Because no additional operations are necessary once the semiconductor is deposited, this provides the added benefit of keeping a clean semiconductor dielectric interface. This structure, exposes the semiconductor to ambient conditions, which may hasten breakdown due to oxygen, water, and other reasons. Despite these structural disadvantages, remarkable progress has been made in improving the charge carrier mobility of organic semiconductors over the past decades, particularly in the last few years, especially with the development of new materials, improved materials processing, and device architecture optimization.

An OFET is made up of many functional layers. Evaporated small-molecule, solution-cast polymers produce an organic semiconducting layer, which is a charge transport layer through which electric current flows. For simulation, pentacene is used as an organic semiconducting layer with thickness 25 nm and is deposited on the gate dielectric as shown in Fig. 3. Pentacene is a common organic semiconductor with a HUMO-LUMO bandgap energy of 2.25 eV. Thickness of gate dielectric is taken as 5.3 nm which is of 3.6 nm aluminum oxide layer and 1.7 nm SAM layer of n-tetradecyl phosphonic acid offering capacitance density of 600 nF/cm^2 [16]. To define source/drain (S/D) electrodes, metal contacts were placed on the top. The width (W) and length (L) of this device depiction were 100 µm and 30 µm, respectively. The geometry used for this device simulation is BGTC.

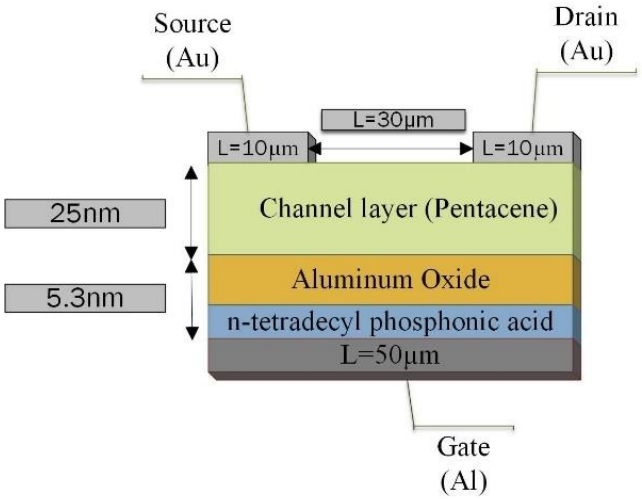

Fig. 3. Schematic Representation of pentacene OFET 2D BGTC structure used in simulation [16] (color online)

Table 1. The OFET parameters used in the 2D device simulation

Sl. No.	Parameters	Symbol	Values	Units
01.	Channel length	L_g	30	μm
02.	Thickness of Active layer	$T_{pentacene}$	25	nm
03.	Dielectric thickness	T_{OX}	5.3	nm
04.	Energy bandgap	E_g	2.25	eV
05.	Electron affinity	E_a	2.49	eV
06.	Intrinsic p-type doping	n_i	2×10^{17}	cm^{-3}
07.	Work function of Al gate	$\emptyset_g$	4.1	eV
08.	Work function of (S/D) Au	$\emptyset_c$	5.1	eV
09.	Acceptor like states density at the edge of conduction band	N_{TA}	9×10^{12}	$cm^{-3}eV^{-1}$
10.	Donor like states density at the edge of valance band	N_{TD}	4.5×10^{12}	$cm^{-3}\ eV^{-1}$
11.	Characteristics decay energy of tail distribution for acceptor like state	W_{TA}	0.3	eV
12.	Characteristics decay energy of tail distribution for donor like state	W_{TD}	0.5	eV
13.	Characteristics decay energy of gaussian distribution for acceptor like states	W_{GA}	0.15	eV
14.	Characteristics decay energy of gaussian distribution for donor like states	W_{GD}	0.15	eV
15.	Gaussian peak energy distribution	E_{GA}	0.5	eV
16.	Electron mobility	μ_n	7×10^{-4}	$cm^2/V\text{-}s$
17.	Hole mobility	μ_p	0.54	$cm^2/V\text{-}s$
18.	Pool Frenkel factor	BETAP.PFMOB	7.758×10^{-8}	$eV(V/cm)^{1/2}$
19.	Zero-Field activation energy	ΔE_a	1.792×10^{-7}	eV

3. Derivation of charge density and physical equation

Numerical simulation is an effective technique for learning about the physics of electrical devices and materials. It is also a low-cost and effective technique for optimizing the design and operation of semiconductor devices. ATLAS was used to design the OFET device structure, and its electrical characteristics were simulated. This software is based on a set of fundamental equations that are related to performance parameters. The ATLAS utilized Poisson's equation and the Continuity equation to simulate and measure its properties [17].

Poisson's equation [18] connects electrostatic potential fluctuations to local charge densities. The following mathematical relationship describes it:

$$\nabla . E = \frac{\rho}{\epsilon} \tag{1}$$

In equation (1),
ρ- charge density
ϵ- permittivity

$$\rho = q\,[\,p - n + N_D^{+} - N_A^{-}] \tag{2}$$

Here in equation (2),
N_D^{+}- ionization donor density
N_A^{-}-ionization accepter density
p - hole concentration,
n - electron concentration.

Equations (3) and (4) illustrate the continuity equations for electrons and holes that characterize the time-dependent behavior of charge carrier propagation [19].

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla . Jn + Gn - Rn \tag{3}$$

$$\frac{\partial p}{\partial t} = \frac{1}{q}\nabla . Jp + Gp - Rp \tag{4}$$

Here in equations (3) and (4), *Jn* and*Jp* are electron and hole densities, *Gn (Rn)* and *Gp (Rp)* are electron and hole generation (recombination) rates, and q is the basic electronic charge. Drift-diffusion equations are a third significant set of equations for explaining charge carrier device physics.

$$J_p = qn\mu_p E_p - qD_p\nabla_p \tag{5}$$

$$J_n = qn\mu_n E_n + qD_n\nabla_n \tag{6}$$

Parameters from equations (5) and (6) are,
μ_n– electron mobility
μ_p- hole mobility
D_n -electron diffusion constant
D_p - hole diffusion constants
E_n- electron electric fields
E_p- hole electric fields

For numerical modelling of an OFET device in which charge transport happens as a result of charge carrier hopping between localized states. The Poole-Frenkel mobility model [20] was used to characterize the dependency of mobility at high electric fields in a pentacene active channel. The mobility free field is provided by equation (7) [28].

$$\mu_0 = \frac{qv_0}{kT}\eta_t^{-2/3} exp\left[-2k\left(\frac{3X}{4\pi\eta_t}\right)^{1/3}\right] \tag{7}$$

where v_0 represents the attempt to jump frequency, the percolation constant is represented by X, k is the reciprocal of the radius of career localization, and the effective transport energy is represented by η_t. ATLAS simulations included thermionic emission and Poole-Frenkel barrier reduction. Equation gives the field dependent mobility (8) [27].

$$\mu(E) = \mu_0 exp\left[\frac{\Delta E_a}{kT} + \left(\frac{\beta}{kT} - \gamma\right)\sqrt{E}\right] \tag{8}$$

In the following equation,
μ_0- zero field mobility
ΔE_a - zero field activation energy
β - Poole-Frenkel factor
γ- Fitting parameter

Various defect states exist in the bandgap of disordered organic semiconductor materials, trapping charge carriers. Poisson's equations are changed to account for trapped charge by including an extra term Q_T in equation (9) which represent trapped charge [21].

$$\rho = q\,(p - n + N_D^{+} - N_A^{-}) + Q_T \tag{9}$$

where $Q_T = q\,(p_t - n_t)$,
p_t- ionized density of donor like traps
n_t- ionized density of accepter like traps

The density of the defect states (DOS) g(E), which dominates the characteristics of amorphous or polycrystalline TFTs, is represented by four components from equations (10-13):

$$g_{TA}(E) = N_{TA}\exp\left[\frac{E - E_c}{W_{TA}}\right] \tag{10}$$

$$g_{TD}(E) = N_{TD}\exp\left[\frac{E_v - E}{W_{TD}}\right] \tag{11}$$

$$g_{GA}(E) = N_{GA}\exp\left[-\left[\frac{E_{GA} - E}{W_{GA}}\right]^2\right] \tag{12}$$

$$g_{GD}(E) = N_{GD}\exp\left[-\left[\frac{E - E_{GD}}{W_{GD}}\right]^2\right] \tag{13}$$

E - trap energy
E_c- conduction band energy
E_v- valance band energy

DOS is defined for exponential tails by its acceptor and donor similar states in the tail distribution at conduction (N_{TA}) and valence band edge (N_{TD}), as well as its attenuation energy (W_{TA} and W_{TD}). For gaussian

distributions, DOS is characterized by its total state density (N_{GA} and N_{GD}), typical attenuation energy (W_{GA} and W_{GD}), and peak energy distribution (E_{GA} and E_{GD}). Because pentacene-based OFET is a P-type, we only look at donor-like states [22] – [24]. As a result, g(E) is given as

$$g(E) = g_{TD}(E) + g_{GD}(E) \quad (14)$$

and the trapped charge η_T is given by:

$$\eta_T \int_{E_v}^{E_c} g(E).f(E,n,p)dE \quad (15)$$

where *f (E, n, p)* is defined as the ionization probability of donors DOS.

4. Comparison of TCAD simulated and reported results

To calibrate the drain current as in reported data [16] simulation is carried out for long channel length of 30 µm and channel width of 100 µm. The output characteristics are obtained to get optimized results from paper using different models representing FLDMOB (field depending mobility), SRH (Shockley-Read-Hall recombination model) as shown in Fig. 4.

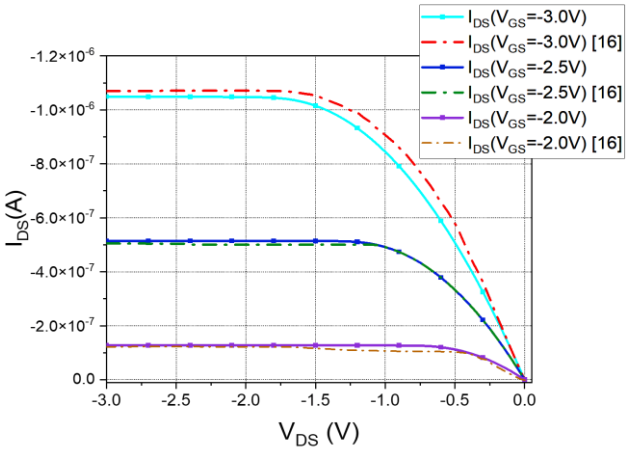

Fig. 4. TCAD simulation of output characteristics matched with the reported data in literature (color online)

From the results in Fig. 4, it can be observed that the results from reported data [16] are matched with the simulated results. The drain current is increased as the gate voltage increases and high drain current at gate voltage -2.5 V is obtained.

5. Results and discussion

To understand the effect of insulator on operation of OFETs, the electrical parameters are assessed from the provided physical structure. The current voltage characteristics are estimated for the various channel lengths and fixed dielectric layer dimensions. Table1 shows the pentacene material properties. The drain current (I_{DS}) is determined by solving equations (16) in a linear area and (17) in saturation.

$$I_{DS} = \frac{W}{L_g}\mu_{FE}C_{ins}(V_{GS} - V_{TH})V_{DS} \quad (16)$$

$$I_{DS} = \frac{W}{L_g}\mu_{FE}C_{ins}(V_{GS} - V_{TH})^2 \quad (17)$$

Here W and L_g are width and channel length respectively, μ_{FE} is field effect mobility, C_{ins} is the gate oxide capacitance per unit area. Fig. 5 and Fig. 6 shows the typical transfer characteristics (I_{DS} - V_{GS}) for drain voltage (V_{DS}) of -3V and Output characteristics (I_{DS}-V_{GS}) for gate voltage (V_{GS}) of -3V. In the results, variation in drain current is observed at different channel lengths (20 µm, 30 µm, 40 µm, 50 µm).

Figs. 5 & 6 depict the output and transfer curves obtained for different channel lengths at a fixed dielectric thickness of 5.3 nm along with fixed dielectric constant of 3.5 which offers capacitance of 600 mF/cm^3 at 30 µm channel length.

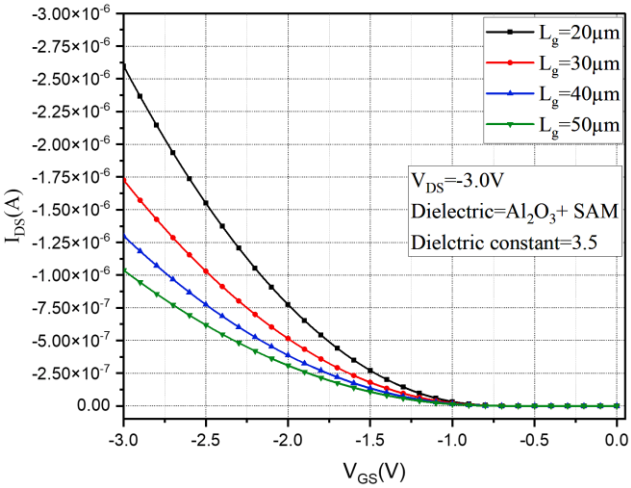

Fig. 5. Transfer curve (I_{DS}-V_{GS}) of OFET with V_{DS} = -3V at different channel lengths (L_g) (color online)

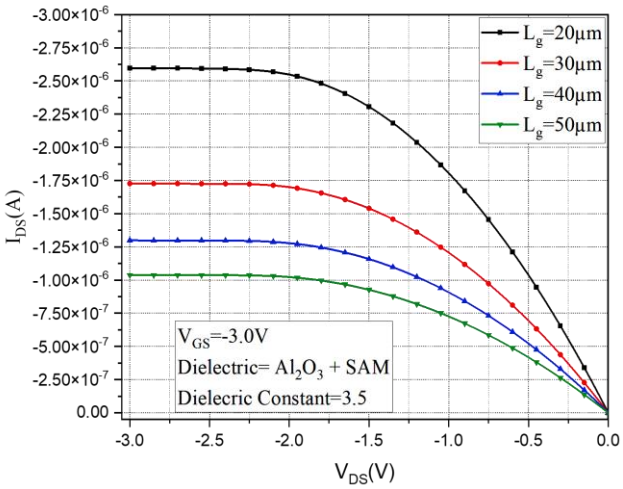

Fig. 6. Output curve (I_{DS}-V_{DS}) of OFET with V_{GS} = -3V at different channel lengths (L_g) (color online)

Table 2. Results obtained from different channel lengths for dielectric constant 3.5

Channel Length (μm)	Dielectric thickness	V_{TH} (V)	SS (V/dec)	I_{on}/I_{off}
20	5.3 nm	-1.20	0.11	3.29×10^5
30	5.3 nm	-1.41	0.11	9.47×10^5
40	5.3 nm	-1.39	0.11	3.30×10^5
50	5.3 nm	-1.48	0.11	9.51×10^5

From the Table 2 above, parameters obtained from the transfer curve are V_{TH}, SS, I_{on}, I_{off}, I_{DS} at V_{GS}=-3.0V and current ratio is improved as with decreasing channel length at fixed dielectric thickness.

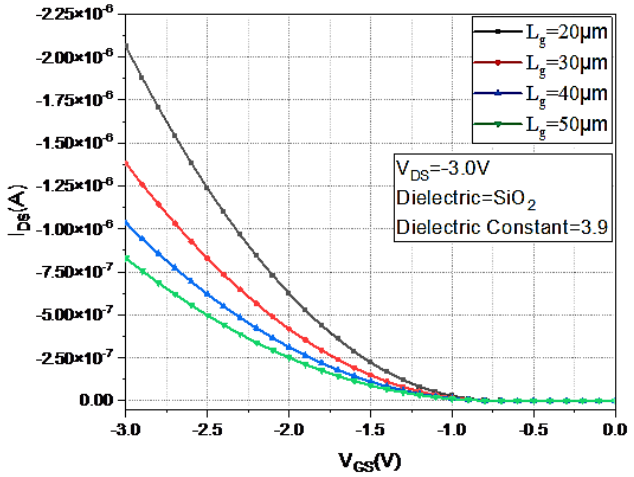

Fig. 7. Transfer curve (I_{DS}-V_{GS}) of OFET with V_{DS} = -3V at different channel lengths (L_g) with SiO_2 as dielectric (color online)

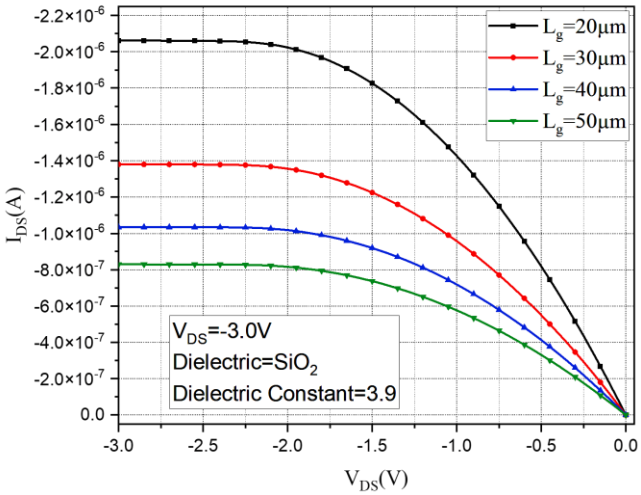

Fig. 8. Output curve (I_{DS}-V_{DS}) of OFET with V_{GS} = -3V at different channel lengths (L_g) with SiO_2 as dielectric (color online)

Table 3. Results obtained from different channel lengths for SiO_2 as dielectric

Dielectric	Channel Length (μm)	Dielectric thickness	V_{TH}(V)	I_{on}/I_{off}
SiO_2 (3.9)	20	5.3 nm	-1.24	1.16×10^6
SiO_2 (3.9)	30	5.3 nm	-1.43	1.15×10^6
SiO_2 (3.9)	40	5.3 nm	-1.44	4.41×10^5
SiO_2 (3.9)	50	5.3 nm	-1.54	4.42×10^5

From the Table 3 above, improvement in current on off ratio along with increased drain current is observed as the channel length is decreased [25]. The improvement in the (I_{on}/I_{off}) has been observed on decreasing the channel length as charge carriers will take less time to reach drain electrode as shown in transfer and output graphs in Figs. 7 and 8.

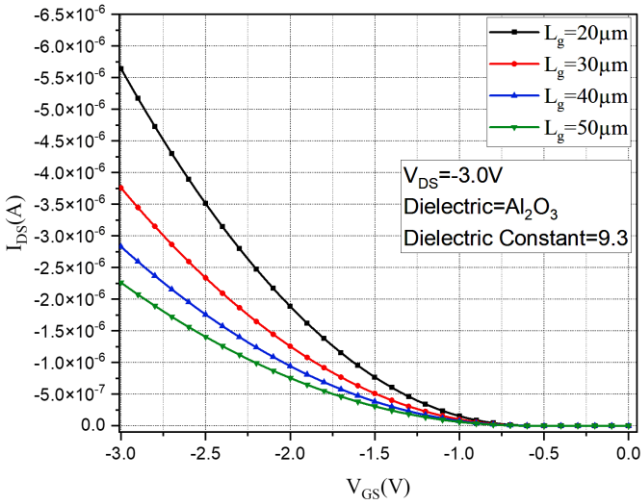

Fig. 9. Transfer curve (I_{DS}-V_{GS}) of OFET with V_{DS} = -3V at different channel lengths (L_g) with Al_2O_3 as dielectric (color online)

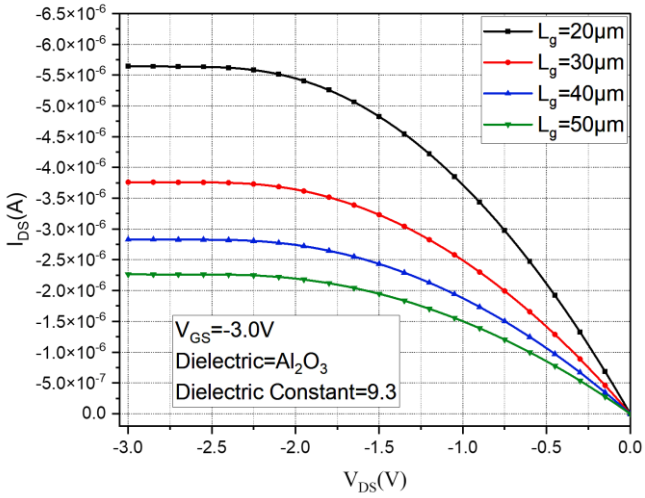

Fig. 10. Output curve (I_{DS}-V_{DS}) of OFET with V_{GS} = -3V at different channel lengths (L_g) with Al_2O_3 as dielectric (color online)

Table 4. Results obtained from different channel lengths for Al_2O_3 as dielectric

Dielectric	Channel Length (μm)	Dielectric Thickness	V_{TH}(V)	I_{on}/I_{off}
Al_2O_3	20	5.3 nm	-0.92	3.72×10^6
Al_2O_3	30	5.3 nm	-0.99	3.73×10^6
Al_2O_3	40	5.3 nm	-1.05	3.74×10^6
Al_2O_3	50	5.3 nm	-1.11	3.75×10^6

In the Table 4 above, Al_2O_3 is taken as a dielectric material with dielectric constant 9.3 which provides better results than the SiO_2 dielectric material. Transfer characteristics (Fig. 9) depicts improved V_{TH} of -0.99, SS value of 0.083, current on/off ratio up to 10^6 and high drain current value at 20 μm and 30 μm channel lengths. This improvement in transfer and output characteristics (Figs. 9 and 10) is observed due to increase in dielectric constant value which in turn increases C_{ins} (increase of injection of free carriers).

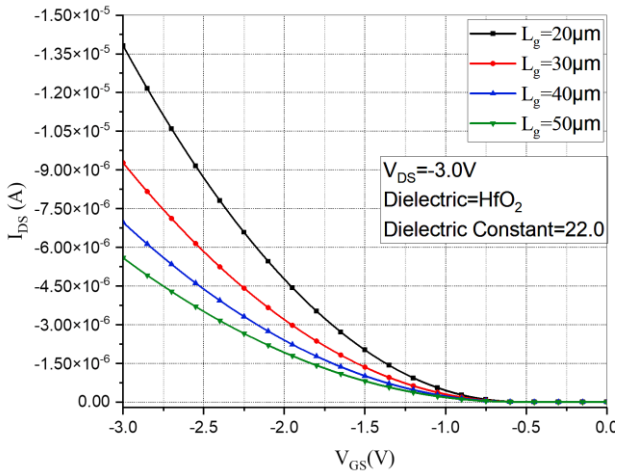

Fig. 11. Transfer curve (I_{DS}-V_{GS}) of OFET with V_{DS} = -3V at different channel lengths (L_g) with HfO_2 as dielectric (color online)

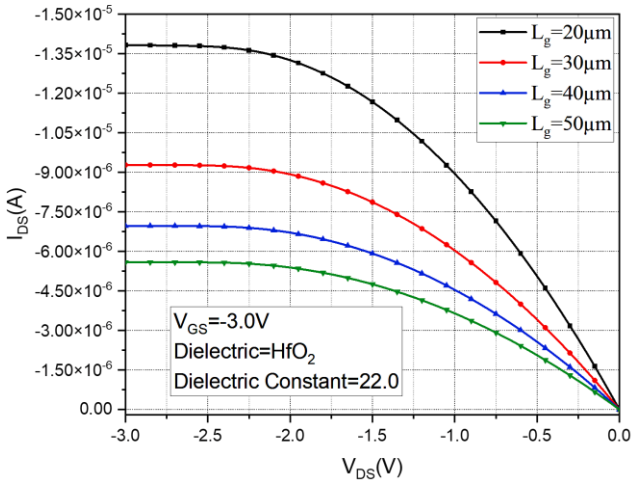

Fig. 12. Output curve (I_{DS}-V_{DS}) of OFET with V_{GS} = -3V at different channel lengths (L_g) with HfO_2 as dielectric (color online)

Table 5. Results obtained from different channel lengths for HfO_2 as dielectric

Dielectric	Channel Length (μm)	Dielectric Thickness	V_{TH} (V)	I_{on}/I_{off}
HfO_2	20	5.3 nm	-0.75	2.31×10^7
HfO_2	30	5.3 nm	-0.85	2.32×10^7
HfO_2	40	5.3 nm	-0.92	2.33×10^7
HfO_2	50	5.3 nm	-0.88	1.42×10^7

Further Figs. 11 and 12 show the transfer and output curves of pentacene OFET for different channel lengths at HfO_2 (k=22) and at gate voltage (V_{GS}=-3.0V). The increase dielectric constant gave an improved results with SS=0.0705 V/dec, current on off ratio of 2×10^7 and high drain current value of 1.39×10^{-5} A at 20 μm channel length. This large gain in device performance is attributed to an increase in drain current.

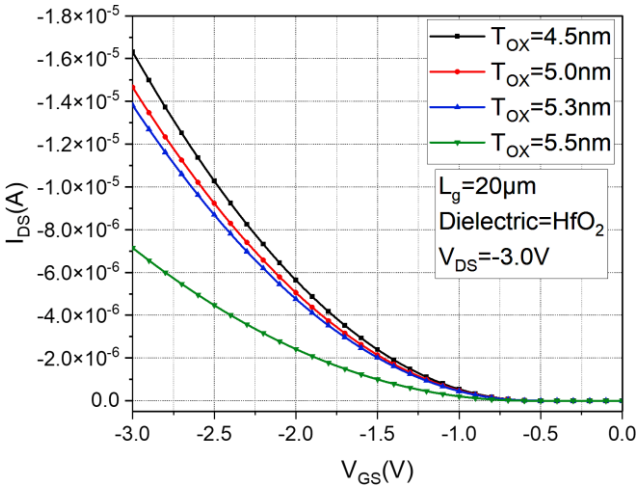

Fig. 13. Transfer curve (I_{DS}-V_{GS}) of OFET with V_{DS} = -3V at different dielectric thickness (T_{OX}) with HfO_2 as dielectric (color online)

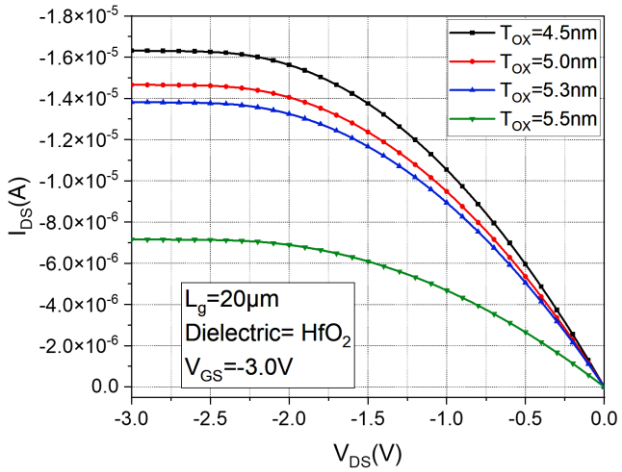

Fig. 14. Output curve (I_{DS}-V_{DS}) of OFET with V_{GS} = -3V at different dielectric (T_{OX}) with HfO_2 as dielectric (color online)

Table 6. Results obtained from above curves for different dielectric thickness

Dielectric	Channel Length (μm)	Dielectric Thickness	V_{TH} (V)	I_{on}/I_{off}
HfO_2	20	4.5 nm	-0.73	1.74×10^7
HfO_2	20	5.0 nm	-0.74	2.48×10^7
HfO_2	20	5.3 nm	-0.75	2.31×10^7
HfO_2	20	5.5 nm	-0.86	5.54×10^6

Further Table 6 shows the results obtained from graphs from Figs. 13 and 14 for different dielectric thickness values. The drain current starts increasing linearly with increase in V_{DS} at constant voltage V_{GS} = -3.0 V. The decrease in dielectric thickness gives results similar to effects of increasing dielectric value of dielectric layer without actually changing material [26]. The significant improvement in the device performance is observed due to increase in drain current. But for 5.5 nm dielectric thickness we get very less drain current value of 7.14×10^{-6} A.

6. Conclusion

The electrical properties of an OFET have been modelled. This work presents a 1-D analytical as well as a 2-D simulation for the intrinsic or light doped organic semiconductor. Open surface configuration in organic transistors, allows to determine the transfer and output characteristics for each gate voltage. Thereafter, the effect of dielectric materials like SiO_2, Al_2O_3 and HfO_2 on OFET characteristics is investigated using Silvaco TCAD with fixed dielectric thickness of 5.3nm and variable channel length is measured. It has been observed that various device performance parameters are affected by changing channel length. Though a steady decrease in channel length improves drain current and gate capacitance per unit area. High-k dielectric materials (Al_2O_3 and HfO_2) provided high drain current, low threshold voltage current ratio as well as good Sub-threshold slope value as compared to low k dielectric materials. After optimizing device for fixed dielectric thickness, it is found that HfO_2 gives better results so thereafter we varied dielectric thickness from 4.5 nm to 5.5 nm and found that 4.5 nm thickness dielectric provided high drain current and this device can be further used as sensor as well as transistor for low voltage applications which will provide less fabrication cost along with less fabrication steps.

Acknowledgment

We thank VLSI research group, Department of Electronics and Communication Engineering NITTTR Chandigarh for their interest in this work and useful comments to draft the final form of the paper. We would like to thank NITTTR Chandigarh for lab facilities and research environment to carry out this work.

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