DC and switching performance of normally-off 4H-SiC TI-VJFET

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Vertical-Junction-Field-Effect-Transistors (VJFETs) are currently the most mature 4H-SiC devices for high power/temperature and switching application. In this paper, DC and switching characteristics of TI-VJFETs has been studied using 2D Sentaurus TCAD with variation of channel width (0.81~0.93 μm), gate-drain capacitance (1~50 pF) and temperature (RT~200^{0}C). It was found that increase in channel width forward current increase from 3.99 A to 5.77 A due to decrease in on-resistance with increase in conduction path while blocking voltage decrease from 850 V to 175 V due to decrease in depletion region width. For switching analysis, switching time and energy loss increase with increase in gate – drain capacitance. For temperature increase RT to 200^{0}C, turn-on and energy loss (3~ 5 ns & 1.8~3 μJ) increased while turn-off and energy loss (9~6ns & 5.4 ~3.6 μJ) decreased.

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1. Introduction

The wide bandgap materials based power devices have low power losses, more efficient, fast and reliable, operating at higher temperature and compact in size. 4H-SiC normally-off TI-VJFET power semiconductor devices are most attractive and promising device for high power, efficiency, temperature and fast switching applications due to its high critical electric field, high saturation drift velocity, low on-resistance, simple fabrication techniques and direct fail safe shield to high power systems [1].

The switching losses turn-on and turn-off TI-VJFET depends on channel width, channel doping concentration, gate resistance, capacitance and gate driver applied voltage. Different design structures such as Trenched and Implanted, Source Inserted Double gate structure, buried grid, different gate drive circuit, cascade circuit to improve the switching time and energy losses of VJFET. A normally-off 4H-SiC trenched and implanted VJFET was fabricated [2] and measured a very low specific resistance of 3.6 mΩcm^2 with a blocking voltage of 1726 V. The drift thickness was 9.4 μm and doped to $7\times10^{15}\ cm^{-3}$. The channel width was 0.55 μm, with same doping density as drift layer. The rise time of 118 ns and fall time of 110 ns was measured. The switching transients were also performed at room temperature up to 200 °C [3], the turn-on and turn-off times were less than 10 ns at all temperatures from RT – 200 °C. The turn-on losses increased and turn-off losses decreased for increasing temperature from RT to 200 °C. A 10 nF capacitor was also used with gate driver to increase the switching speed. This was the fastest switching speed reported to date on any normally-off SiC JFETs.

In this paper, The effect of vertical channel width W_{Ch} on I-V and blocking characteristics has been studied. The switching behavior of the device with different parameters such as gate to drain capacitance C_{GD} and temperature range from 25 °C to 250 °C has been examined. Finally,turn-on and turn-off time and switching losses are calculated.

2. Proposed structure and models

Fig. 1 shows schematic view of 4H-SiC TI-VJFET structure, n-type vertical channel and drift layer having a doping concentration of 5×10^{15}cm^{-3} respectively.The vertical channel width varies (0.81-0.93μm) while gate-drain capacitance (10-50 pF). Gate is p-type doped 2.3×10^{17}cm^{-3} above this gate there is a layer of highly doped P^{++} layer for reliable ohmic contact. Both drain and source regions have n-type doping of 1×10^{18}cm^{-3}. The following models have been used for DC and switching analysis, Shockley-Read-Hall (SRH) and Auger recombination model, Avalanche generation, Bandgap narrowing, Impact ionization, Incomplete ionization model [4].

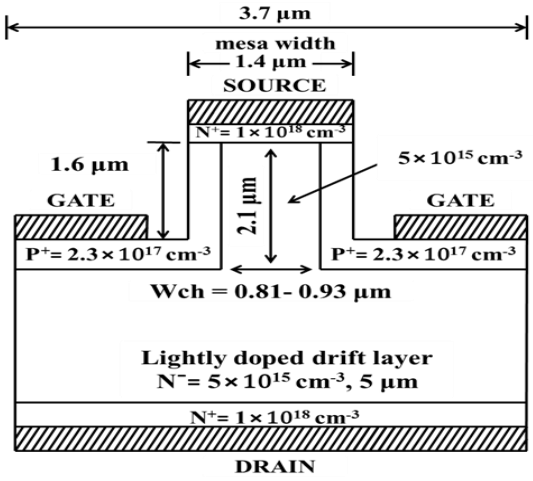

Fig. 1. A cross-sectional view of TI-VJFET.

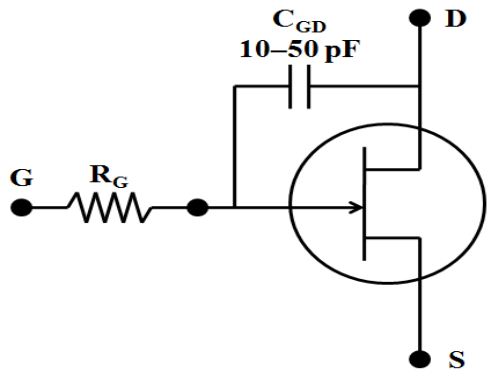

Fig. 2. Circuit diagram of TI-VJFET with different values of C_{GD} .

3. Results and discussion

3.1 DC characteristics

The TI-VJFET is normally-off, hence no drain to source current flows at zero gate bias. When gate to source voltage is increased from zero, the depletion layer between channel and gate region shrinks, and hence the drain to source current increases [5]. Fig. 3 shows the channel width was varied from 0.81 µm to 0.93 µm while the gate voltage varies 2 to 2.5V. The results indicates that increase in channel width, drain current increase from drain to source 3.99 to 5.77 A due to decrease in channel on-resistance with increase in conducting path. A very low on-resistance of 0.39 mΩcm^2 was calculated at (V_G @2.5 V & I_{DS} @3.99 A).

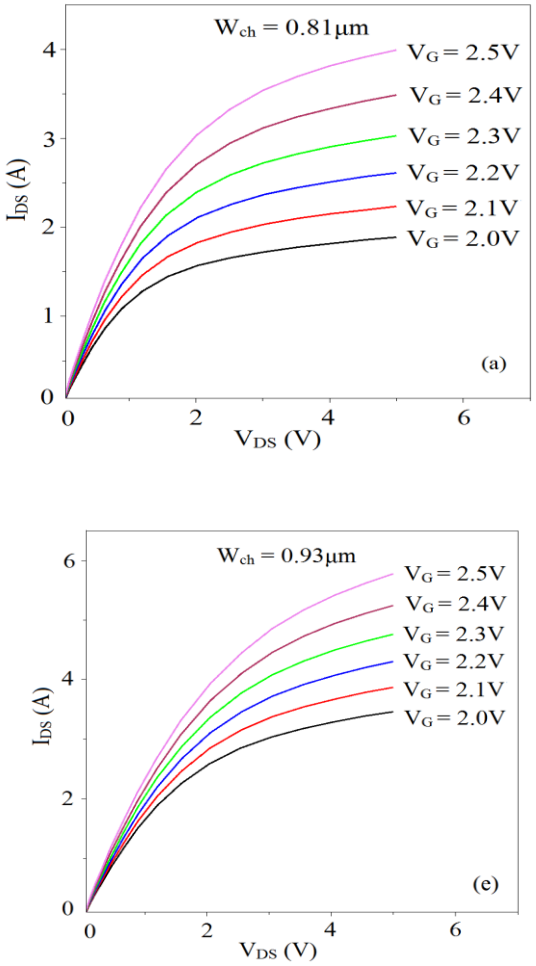

Fig. 3. Forward I-V characteristics of TI-VJFET at channel width 0.81&0.93 µm.

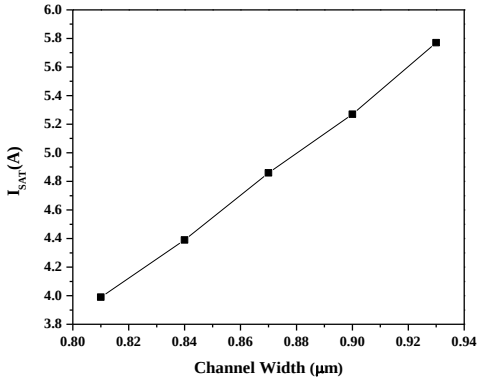

Fig. 4. Variation of drain current with different values of channel width @ V_g = 2.5 V.

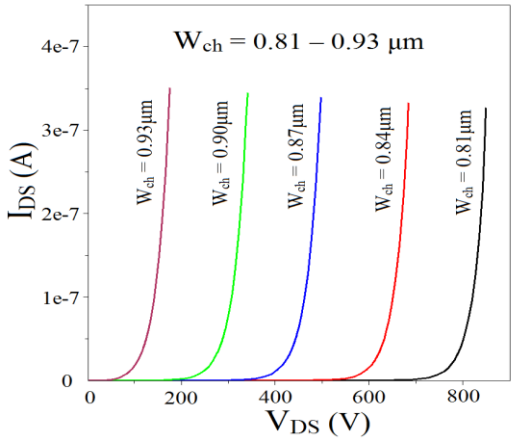

Fig. 5. Variation of blocking voltage with channel width W_{CH}.

The blocking voltage of device is very important because it determines the maximum limit up to which device behaves normally, if the voltage exceeds this limits the avalanche breakdown takes place and high current produce and hence the device performance degrade. Fig. 5 shows variation of blocking voltage from 850 ~175 V with channel width 0.81~0.93 µm. As the channel width increase, blocking voltage decreases due to decrease in depletion region width.The high blocking voltage device shows smaller gate to drain junction capacitance [6]. Therefore, for faster switching performance of the device the channel width of 0.81 µm has been selected because at this value maximum blocking voltage of 850 V was calculated.

3.2 Switching characteristics

The switching time of the device depends on the charging and discharging time of the input capacitances. Faster the input capacitance are charged and discharged, faster the turn-on and turn-off of the device. Different types of parasitic elements are present in the TI-VJFET device structure. Two p-n diodes D_{gs} and D_{gd} are formed between gate to source and gate to drain regions respectively. The diode D_{gs} plays an important role during the device on state. And the diode D_{gd} remains reversed biased due to the higher value of drain voltage compared to the gate voltage. Parasitic capacitances C_{gd} and C_{gs} are present between gate to drain and gate to source terminals. The device turn-on and turn-off time, depend on the charging and discharging time of gate to drain capacitance C_{gd} [7]. The variation of switching time with different values of C_{gd} (1pF to 50 pF) at 400 V V_{DS} bus voltage is shown in Fig.6. As expected the switching times turn-on and turn-off increased by increasing the C_{gd} [8]. The turn-on times of 6 ns and turn-off times of 20 ns was recorded at C_{gd} of 50pF.

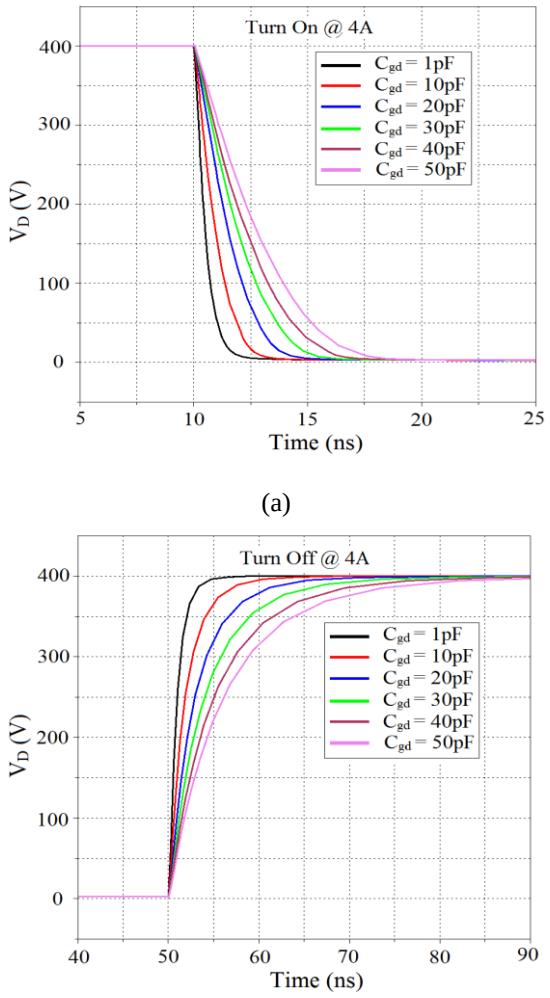

Fig. 6. Variation of switching times @ 400 V with different values of C_{gd} and R_g = 10 Ω. (a) Turn-On (b) Turn-Off.

The temperature dependent switching characteristics of TI-VJFET are investigated. The switching time was calculated at room temperature upto 200 ºC shown in Fig. 7. As expected [9,10] turn-on time increases while turn-off time decreases with the increase in temperature. At high temperature, free carriers are generated which accumulate near the gate region and therefore increased the gate to drain capacitance consequently turn-off time decreases. Table 1 shows switching time and energy losses at RT and 200 ºC. As the temperature increases upto 200 ºC, turn-on time increased from 3 ns to 5 ns and turn-off time decreased from 9ns to 6ns while the turn-on energy loss increased from 1.8 µJ to 3 µJ and turn-off energy decreased from 5.4 µJ to 3.6 µJ. The simulated results are in agreement with the experimental work [9]. The simulated results indicates that the normally-off 4H-SiC TI-VJFET shows fastest switching speed and lowest switching losses reported to date on any normally-off SiC VJFETs.

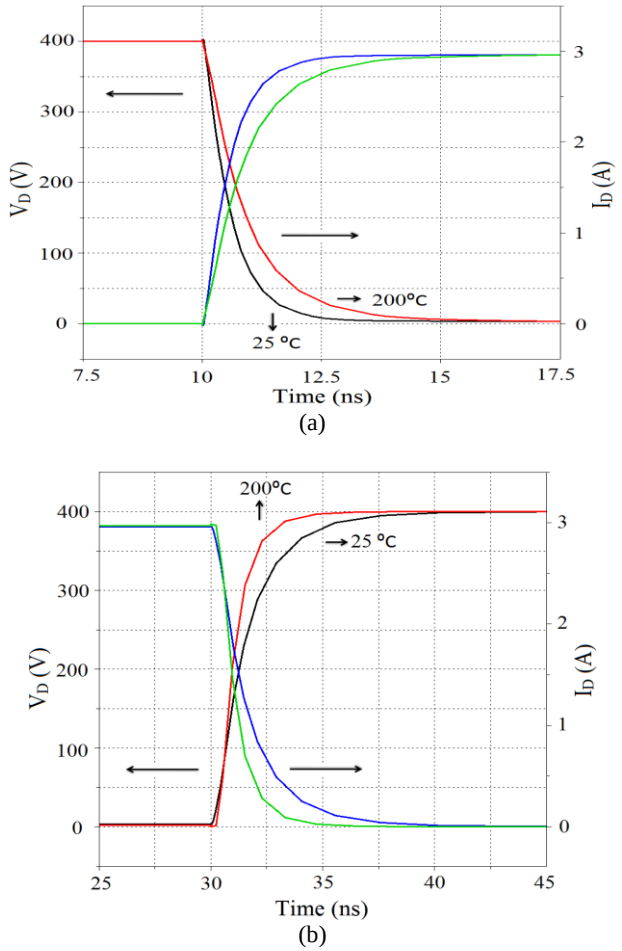

Fig. 7. Variation of switching times with temperature @ 3 A. (a) Turn-On (b) Turn-Off.

Table 1. Calculation of switching time and energy at different temperature.

Sr. no.	Temperature (^{0}C)	T_{ON} (ns)	T_{OFF} (ns)	E_{ON} (µJ)	E_{OFF} (µJ)
1	25	3	9	1.8	5.4
2	200	5	6	3	3.6

4. Conclusion

DC and switching characteristics of 4H-SiC TI-VJFETs was studied with variation of channel width (0.81~0.93 µm), gate-drain capacitance (1~50 pF) and temperature (RT~200 °C) using 2D Sentaurus TCAD. It was found that as the channel width increases forward current also increases due to decrease in on-resistance with increase in conduction path, while blocking voltage decrease due to depletion region width decreases. For switching analysis, switching time and energy losses increase with increase in gate –drain capacitance. While with temperature increase, turn-on time and energy losses increased, while turn-off time and energy losses decreased. The simulated results shows fastest switching speed and lowest switching losses reported to date on any normally-off SiC VJFETs.

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