Current-voltage (*I-V*) characteristics of Au/InGaAs/n-GaAs Schottky barrier diodes

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In this study, the forward and reverse bias current-voltage (*I-V*) characteristics of Au/InGaAs/n-GaAs Schottky barrier diodes (SBDs) have been investigated at room temperature. InGaAs epilayer was grown on (100) oriented n-GaAs substrate using V80-H solid source Molecular Beam Epitaxy (MBE) system. Atomic Force Microscope (AFM) was used in order to study the surface properties of InGaAs epilayer. The AFM measurement was performed by using an Omicron variable temperature STM/AFM instrument. The electrical parameters such as barrier height (Φ_b), ideality factor (n), series resistance (R_s) and interface states (N_{ss}) of Au/InGaAs/n-GaAs SBDs have been calculated by using forward and reverse bias *I-V* measurements. The energy distribution of interface states of the structure was obtained from the forward bias *I-V* measurements by taking the bias dependence of the effective barrier height (Φ_e) into account. In addition, the values of R_s and Φ_b were determined by using Cheung's methods and results have been compared with each other.

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1. Introductıon

III-V group semiconductors, such as Gallium Arsenide (GaAs)-based structures, are used in the research and development of optoelectronics and microelectronics devices [1-7]. There are a lot of GaAs-based structure growth techniques such as Chemical vapor deposition (CVD) [8], Metal organic chemical vapor deposition (MOCVD) [7] and MBE [9-10]. Among these techniques, MBE can be used to grow samples in a high vacuum, which is important when preparing high quality samples. In addition, the reflection high energy electron diffraction (RHEED) technique has been widely applied to the study of this system. The reconstruction and growth rate of the surface were determined by RHEED oscillations [9-10].

Recently, there are many contact studies on GaAs-based structures [1,3,4,7,11-16]. Metal-Semiconductor (MS) contacts are important research tools in the characterization of new semiconductor materials and at the same time the fabrication of these structures plays a crucial role in constructing some useful devices in technology. Schottky barrier diodes which are of the most simple of the MS contact devices have an important role in the semiconductor technology. The performance of SBDs depends on such electrical parameters as ideality factor, barrier height formation at M/S interface, series resistance and interface states. Electronic properties of SBDs are characterized by these parameters. There are recently a vast number of reports of experimental studies of these characteristics parameters in a great variety of MS contacts [15-23].

In the present work, the experimental forward and reverse *I-V* characteristic of Au/InGaAs/n-GaAs SBDs was investigated at room temperature. Φ_b, n, R_s and N_{ss} were extracted from forward bias *I-V* measurements. In addition, Φ_b and R_s values were determined by using Cheung's method [24]. It was seen that there was a good agreement between the values obtained from *I-V* measurements and Cheung's method. Moreover, AFM was used in order to study the surface properties of InGaAs epilayer.

2. Experimental procedure

The InGaAs epilayer was grown on (100) oriented n-GaAs substrate using V80-H solid source MBE system. Prior to growth, the substrate was cleaned using acetone, methanol and deionized water for the removing of the organic impurities. In MBE system, firstly GaAs buffer layer with 700 nm thickness was grown on n-GaAs structure to provide the lattice match between the substrate and the epilayers and prevent the migration of defects and the impurities from substrate to the as grown epilayers. The sample was completed by growth of 1000 nm thickness InGaAs epilayer.

For the electrical characterization of the sample, ohmic and rectifier contacts were formed using thermal evaporation system. To form the ohmic contact AuGe/Au metals with the thicknesses of 1100/1000 Å and growth rates of 3.3/3 Å/s were deposited, respectively. After the ohmic contact processes, to form the ohmic contact the sample was annealed at 400 ^{o}C for 3 min in a nitrogen ambient atmosphere. After then, the 2 mm diameter dot shaped rectifier contact was formed by deposition of high purity Au (99.999%) metal with the thickness of 1000 Å and growth rate of 3.9 Å/s.

After the completion of the fabrication of Au/InGaAs/n-GaAs SBDs, current-voltage measurements were performed using Keithley 2400 source-metter. The electrical measurements were made at room temperature and performed using micro computer through an IEEE-488 AC/DC converter card. The schematic diagram of the Au/InGaAs/n-GaAs SBDs is given Fig. 1.

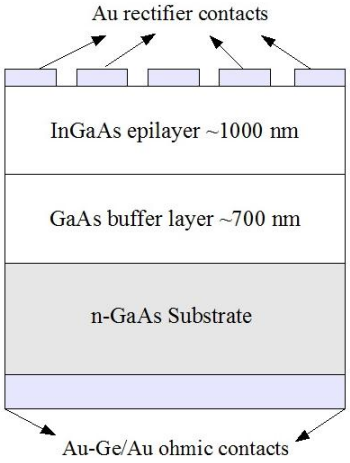

Fig. 1. The schematic diagram of Au/InGaAs/n-GaAs SBDs.

3. Results and discussion

The current-voltage (*I-V*) characteristic of the Au/InGaAs/n-GaAs SBDs is shown in Fig. 2 at room temperature. The experimental *I-V* data were analyzed by the well-known equation at forward bias [25, 26].

$$I = I_o \exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(-\frac{qV}{kT}\right)\right] \tag{1}$$

where q is the electronic charge, k is the Boltzmann's constant, T is the absolute temperature in Kelvin, and I_o is the saturation current which is obtained from the intercept of *lnI* vs *V* curve (Fig. 2) and is expected as

$$I_o = AA^*T^2 \exp\left(-\frac{q\Phi_b}{kT}\right) \tag{2}$$

where A is the effective diode area, A^* is the effective Richardson constant and equals to 8 A cm^{-2} K^{-2} for n-type GaAs.

Once I_o is determined, the Φ_b is obtained by rewriting Eq. (2) as

$$\Phi_b = \frac{kT}{q}\ln\left[\frac{AA^*T^2}{I_0}\right] \tag{3}$$

n is calculated from the slop of the linear region of the forward-bias *lnI-V* plot and is given by

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln I)}\right) \tag{4}$$

Using Eqs. (3) and (4) the values of Φ_b and n of the structure at room temperature were found as 0.65 eV and 4.86, respectively. The value of 4.86 for ideality factor is greater than unity and shows deviation from an ideal diode. This deviation can be attributed wide distribution of low Schottky barrier height patches at M/S interface [27, 28]. In addition, the R_s value was determined from the structure resistance (R_i) vs applied bias voltage (V_i) plot obtained from the *I-V* characteristics where $R_i = dV_i/dI_i$. The R_s of the SBDs at room temperature was found as 4.46 kΩ.

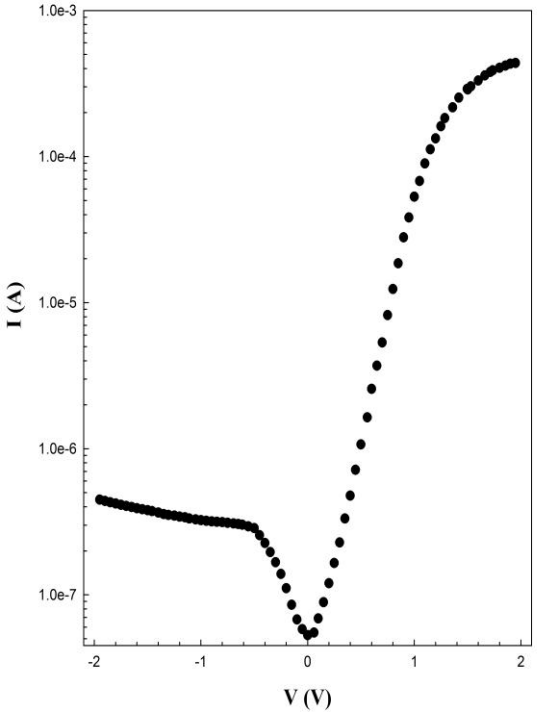

Fig. 2. The forward and reverse bias I-V characteristics of Au/InGaAs/n-GaAs SBDs at room temperature.

The main electrical parameters such as n, Φ_b and R_s were determined using a method developed by Cheung and Cheung [24]. The Cheung's functions given as

$$\frac{dV}{d(\ln I)} = n\left[\frac{kT}{q}\right] + R_s I \tag{5}$$

$$H(I) = V - n\frac{kT}{q}\ln\left[\frac{I}{AA^*T^2}\right] = n\Phi_b + \mathrm{R_s I} \tag{6}$$

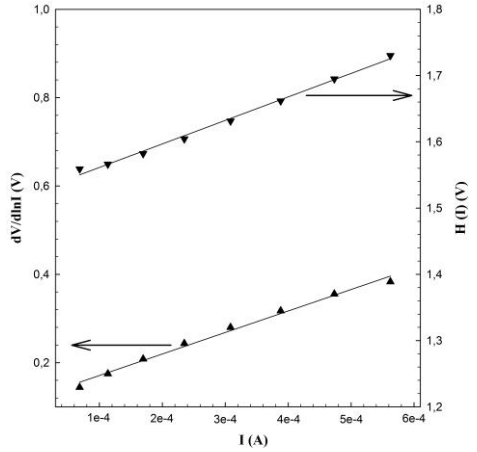

Fig. 3. Experimental dV/dln(I) vs I and H(I) vs I plots of Au/InGaAs/n-GaAs SBDs.

Eqs. (5) and (6) should give a straight line for the data of downward curvature region in the forward bias *I-V* characteristics. Fig. 3 shows the experimental *dV/dlnI* vs *I* and *H(I)* vs *I* plots of Au/InGaAs/n-GaAs SBDs at room temperature. The *n* and R_s values obtained from *dV/dlnI-I* plot was found as 4.73 and 4.87 kΩ, respectively. In addition, the Φ_b and R_s values obtained from *H(I)-I* plot was found as 0.33 eV and 4.35 kΩ, respectively. The R_s values obtained from *dV/dlnI-I* and *H(I)-I* plots are in good agreement with each other and the value obtained from *lnI-V* curve.

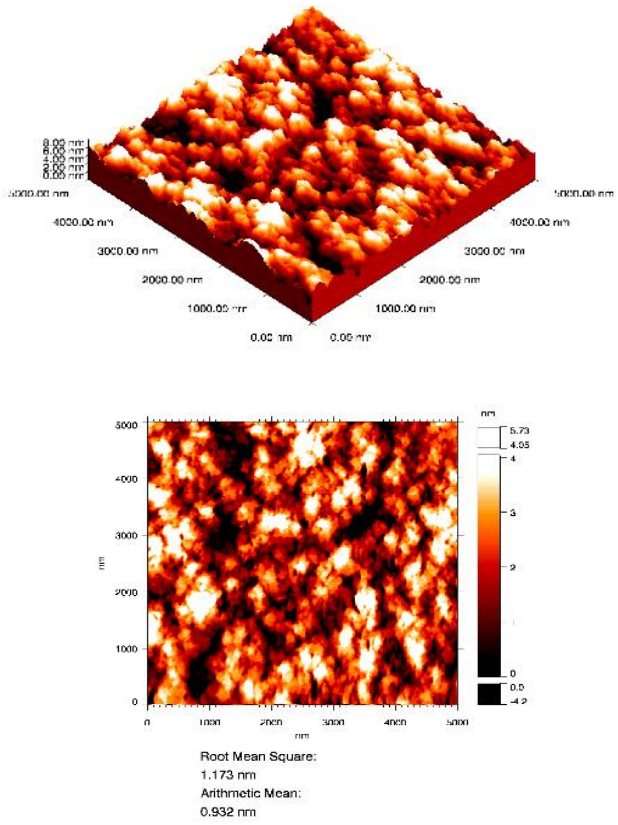

Fig. 4. AFM image with a 5μm×5μm scan area of InGaAs/GaAs structure.

Fig. 4 shows the AFM image with a 5μm×5μm obtained from the InGaAs surface of the sample. As seen from the image, surface of the sample exhibits mounds of varying sizes. As is well known, unstable growth leads the mounded structure on GaAs surfaces due to the step edge barrier that restricts the movement of the adatoms from upper terraces to lower terraces [29-33]. On the other hand, the surface root-mean-square (rms) roughness of the sample is obtained as 1.17 nm over a scan area of 5μm×5μm.

Furthermore, voltage dependent ideality factor (n_V), the effective barrier height (Φ_e) and density of interface states (N_{ss}) can be obtained from following equations, respectively [23].

$$n_V = \frac{qV}{kT\ln(I/I_0)} \tag{7}$$

$$\Phi_e = \Phi_b + \left(1 - \frac{1}{n(V)}\right)(V - IR_s) \tag{8}$$

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_s}{W_D}\right] \tag{9}$$

In n-type semiconductor, the energy of the surface states E_{ss} with respect to the bottom of the conduction band at the surface of semiconductor is given by

$$E_c - E_{ss} = q(\Phi_e - V) \tag{10}$$

The energy distribution profile of N_{ss} as a function (E_c-E_{ss}) for Au/InGaAs/n-GaAs SBDs was extracted from the forward bias *I-V* measurements by taking the bias dependence of the effective barrier height (Φ_e) into account and given in Fig. 5. As can be seen from Fig. 5, there is an exponential decrease from bottom of conduction band towards to midgap of GaAs.

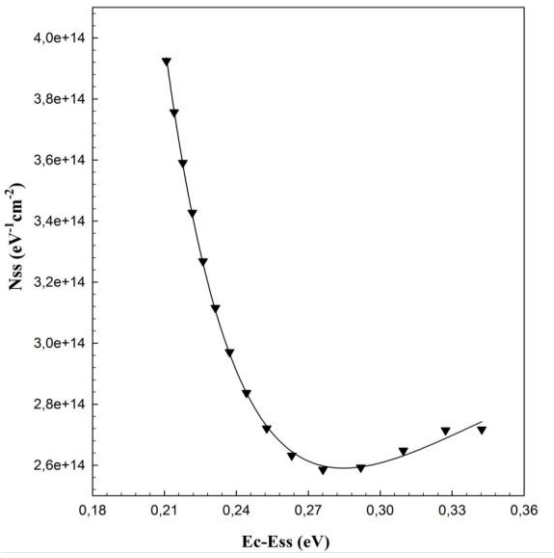

Fig. 5. The energy distribution profile of interface states obtained from the forward bias I-V characteristics of Au/InGaAs/n-GaAs SBDs.

4. Conclusion

Analysis of the forward and reverse bias *I-V* characteristics of Au/InGaAs/n-GaAs SBDs have been investigated at room temperature. The electrical parameters such as barrier height, ideality factor, series resistance and interface states have been extracted from forward bias *I-V* measurement. The values of barrier height, ideality factor and series resistance were determined by using Cheung's methods. It was seen that there is a good agreement between the values of the series resistance and barrier height obtained from *I-V* measurement and two Cheung's plots. The interface states in equilibrium with the semiconductor were calculated from the downward-curvature region in the forward bias *I-V* curves. In conclusion, in our study, surface properties and electrical characteristics of InGaAs/GaAs structure which was grown by using MBE system have been investigated at room temperature.

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