Analytical model of SiC DIMOSFET's drift region voltage impact on current-voltage characteristics

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This paper presents new results obtained by investigations of silicon carbide (SiC) based vertical Double Implanted Metal Oxide Semiconductor Field Effect Transistor (DIMOSFET). The results are described and presented by the analytical model of drift region voltage and it's impact on SiC DIMOSFET current-voltage characteristics. The drift region is devided into sections. For each of them, voltage analytical model across the corresponding section is developed. Mobility dependence model on temperature and electric field is introduced. Finally, current-voltage characteristics are obtained, by using drain to surce voltage model which incorporate the mentioned partial voltages. Proposed model is based on the physics of the SiC DIMOSFET. Significant effects are taken into account, thus the model is accurate. At the same time exposed model is relatively simple. By using developed model simulations were performed. The obtained results are in very good agreement with already known and published ones..

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Keywords: SiC DIMOSFET, Drift region voltage, Analytical model

1. Introduction

The present silicon technology is reaching the material's theoretical limits and cannot fullfil all the requirements of the modern electronics. The semiconductor silicon carbide (SiC) has been identified as a material with the potential to overcome silicon limitations [1-5], because of its superior material advantages such as: large bandgap energy (it depends on polytype: the values for some that are commonly used, are: 2.9 eV for 6H-SiC polytype, 3.25 eV for 4H-SiC polytype and 2.35 eV for 3C-SiC polytype) enables higher junction operating temperatures; high critical breakdown field (approximately eight times that of silicon) permits much smaller drift regions than in standard silicon devices; high electron saturation drift velocity (twice that of silicon); high thermal conductivity (three times that of silicon) permits better heat dissipation [1]. SiC based semiconductor electronic components are presently being investigated and developed for use in high-power, high-temperature, high-frequency and high-radiation conditions under which conventional semiconductor components cannot adequately perform [1-5]. High voltage and high current potentiality of SiC based devices has been proved, and ability to operate at high temperatures have been reported as well [5].

MOSFET is one of the most frequently used electron devices [7]. Si power MOSFETs are very popular in power electronics (often used as switching devices) dominantly because: their MOS gate drives are well insulated and require little drive signal power; these devices are ″normaly off ″ (unbiased gate – there is no current). In the power switching area, SiC based unipolar devices have now surpassed the theoretical limits for Si devices by wide margins, for example more then ten times for power MOSFET [1]. Their sizes are nearly twenty times smaller than correspondingly rated Si based devices [1]. SiC can be thermally oxidized to produce SiO_2 [1, 7, 8], thus it is possible to fabricate a variety of MOS based devices in the material. Bearing in mind mentioned advantages of SiC, SiC MOSFETs could replace Si ones, specially for use in power electronics and to operate under extreme conditions. It should be mentioned that there are two main electrical deficiencies of SiC MOSFETs compared to Si MOSFETs: effective inversion channel mobilities in most SiC MOSFETs is much lower (100 cm^2/Vs) than in Si MOSFETs; secondly, SiC oxide is not as reliable as Si oxides, thus SiC MOSFETs are more prone to threshold voltage shift, gate leakage and oxide failures than comparably biased Si MOSFETs. Nevertheless, thanks to very good characteristics, SiC MOSFET can successfully be employed as a power electronic devices. This components can be used in different sofisticated systems which work under extreme conditions.

In this paper, analytical model for drift region voltage, of a vertical DIMOSFET, is presented. The proposed model is based on a SiC vertical DIMOSFET behaviour. To verify developed model, it is incorporate in I-V characteristics model and simulation were performed.

In Fig. 1 vertical SiC DIMOSFET structure is shown. The model is developed by investigation of carrier's transport which exists in transistor channel (below the oxide layer, within the p-bodies) and marked zones (accumulation and drift).

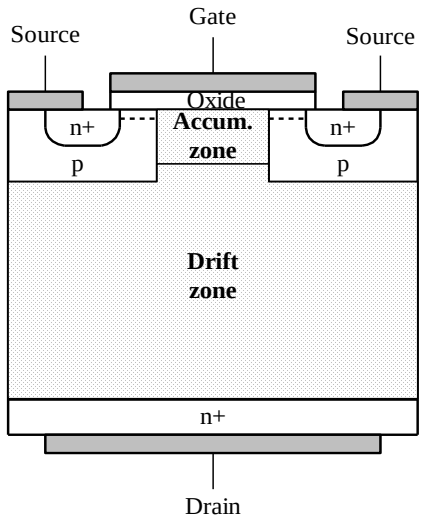

Fig. 1. Cross sectional view of a SiC vertical DIMOSFET structure.

2. Proposed model

Drift-diffusion model of carrier's transport in modern electron devices has remained the most important one. The reason for this approach is the fact that this model strongly relies upon basic concepts of modern transport theory, while at the same time it offers promising capability for construction of models which are simple enough [10, 11].

Carrier's transport in vertical DIMOSFET is dominantly lateral in a channel and dominantly vertical in drift region. With the intention to develop drift region voltage, drift region is divided into two parts: an accumulation zone and a drift zone. Starting from the well known (e.g. [4], [10]) equation for current in the n-type semiconductor bar with the rectangular cross section *W*x*L*:

$$I = qn\mu_n WLE = qn\mu_n WL\frac{dV}{dx} \tag{1}$$

where q is the electron charge, n is the carrier's concentration and μ_n is the carrier's mobility, it is easy to find voltage across the accumulation zone of the examined transistor:

$$V_{Az} = \int_0^{D_{Az}} \frac{I_{Az}}{qn\mu_n WL}dx = \frac{I_{Az}D_{Az}}{qn\mu_n WL} \tag{2}$$

In equation (2) I_{Az} is the current in accumulation zone, x is the vertical (drain to source) direction, D_{Az} is the depth of accumulation region (vertical direction), L is the length (lateral direction) and W the width of accumulation zone.

Similarly, voltage across the drift zone of the examined transistor is:

$$V_{Dz} = \int_{D_{Az}}^{D_p} \frac{I_{Dz}}{qn\mu_n WL}dx + \int_{D_p}^{D} \frac{I_{Dz}}{qn\mu_n W(L+2L_p)}dx = \frac{I_{Dz}}{qn\mu_n WL}(D_p - D_{Az}) + \frac{I_{Dz}}{qn\mu_n W(L+2L_p)}(D - D_p) \tag{3}$$

In equation (3) I_{Dz} is the current in drift zone, D_p is the depth of p-body, L_p is the length of p-body and D is the total thickness of epitaxial layer.

Taking into account voltage across transistor channel V_{ch}, total drain to source voltage can be written in following form:

$$V_{DS} = V_{Az} + V_{Dz} + V_{ch} = V_{drift} + V_{ch} \tag{4}$$

Obviously, current in accumulation zone is the same as current in drift zone. This current equals to the total channel current and transistor current $I_{DS}=I_{Az}=I_{Dz}=I_{ch}$.

Using already known analytical model [2] and bearing in mind that there is, in fact, two channels (shown in Fig. 1. by dashed lines), transistor current in linear operating regime can be written as:

$$I_{DS} = 2\mu_n \frac{W}{L_{ch}} C_{ox}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \tag{5}$$

Introducing developed model (4) in (5), it is obtained:

$$I_{DS} = 2\mu_n \frac{W}{L_{ch}} C_{ox}\left(V_{GS} - V_T - \frac{V_{Az} + V_{Dz} + V_{ch}}{2}\right)(V_{Az} + V_{DZ} + V_{ch}) \tag{6}$$

Transistor current in saturation operating regime can be written as [2]:

$$I_{DS} = \frac{1}{2}\mu_n \frac{W}{L_{ch}} 2C_{ox}(V_{GS} - V_T)^2 = \mu_n \frac{W}{L_{ch}} C_{ox}(V_{GS} - V_T)^2 \tag{7}$$

In equations (5) – (7) $L_{ch}=(L_p-L_n)/2$ is the channel length. It should be mentioned that carrier's concentration, as well as electric field, is dependent on position in transistor ($n=n(x,y)$; $E=E(x,y)$).

Mobility is strongly temperature dependent. It also depends on electric field $\mu=\mu(T,E)=\mu(T,E(x,y))$. This can be modeled as [6], [13], [14]:

$$\mu_n = \frac{\mu_0\left(\frac{T_r}{T}\right)^{\beta} + \frac{v_s}{E_{cx}}\cdot\left(\frac{E(x)}{E_{cx}}\right)^3}{1+\left(\frac{E(x)}{E_{cx}}\right)^4} \tag{8}$$

where μ_0 is the bulk mobility, T_r the room temperature (300 K), T the absolute temperature, β the temperature coefficient with various values used for it, between 1.5 and 2, v_s the carriers saturation velocity and E_{0x} the characteristic value of vertical electric field.

Using (6), (7) and (8), SiC DIMOSFET current-voltage characteristics models can be written as:

- in linear regime:

$$I_{DS}=2\frac{\mu_0\left(\frac{T_r}{T}\right)^{\beta}+\frac{v_s}{E_{cx}}\cdot\left(\frac{E(x)}{E_{cx}}\right)^3}{1+\left(\frac{E(x)}{E_{cx}}\right)^4}\cdot\frac{W}{L_{ch}}C_{ox}\left(V_{GS}-V_T-\frac{V_{Az}+V_{Dz}+V_{ch}}{2}\right)\left(V_{Az}+V_{DZ}+V_{ch}\right) \quad (9)$$

- in saturation regime:

$$I_{DS}=\frac{\mu_0\left(\frac{T_r}{T}\right)^{\beta}+\frac{v_s}{E_{cx}}\cdot\left(\frac{E(x)}{E_{cx}}\right)^3}{1+\left(\frac{E(x)}{E_{cx}}\right)^4}\cdot\frac{W}{L_{ch}}C_{ox}\left(V_{GS}-V_T\right)^2 \quad (10)$$

3. Results and discussion

The model presented in previous section is used for simulations of SiC DMOSFET output current – voltage characteristics. Results are obtained for different polytypes DMOSFETs. In the simulations, the transistor dimensions are taken as constants. The following values are used: for the channel width W = 700 μm, for the channel length L = 4 μm, for the thickness of gate oxide t_{ox}=50 nm, for the dielectric constant of oxide ε_{ox} = 3.82 ε_0, for the dielectric constant of SiC ε_{SiC} = 9.7 ε_0.

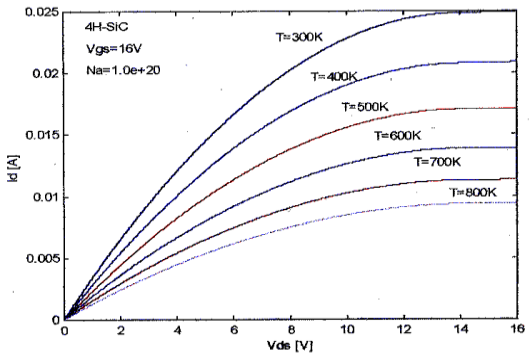

Fig. 2. 4H-SiC DMOSFET output characteristics, for different temperatures, V_{GS}=16V, N_a=10^{20}m^{-3}.

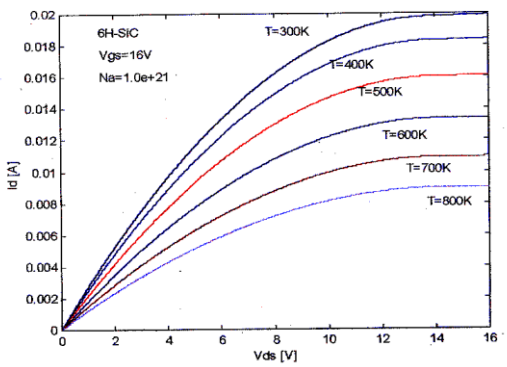

Fig. 3. 6H-SiC DMOSFET output characteristics, for different temperatures, V_{GS}=16V, N_a=10^{21}m^{-3}.

In Fig. 2 output current – voltage characteristics, for 4H-SiC DMOSFET, are given. Presented curves are valid on different temperatures (T=300 K – T=800 K). Values of the used parameters are: gate to source voltage V_{GS} = 16 V and doping concentration N_a=10^{20}m^{-3}.

In Fig. 3 output current – voltage characteristics, for 6H-SiC DMOSFET, are given. Presented curves are valid on different temperatures (T = 300 K – T = 80 0 K). Values of the used parameters are: gate to source voltage V_{GS}=16V and doping concentration is this time N_a=10^{21} m^{-3}.

Observing Figs. 2 and 3, it can be noticed that the drain current is heavily dependent on temperature, under other same operating conditions. Drain current increases when temperature decreases (e. g. for 4H-SiC DMOSFET, in saturation operating regime, transistor current increases from approximately 0.01A on T = 800 K to approximately 0.025A at T = 300 K).

SiC DMOSFET current has also significant dependence on doping concentration when all other operating conditions are kept constant. This is consequence of the fact that the threshold voltage increases when the doping concentration increase

In Figs. 3 and 4 output current - voltage characteristics, for 3C, 4H, 6H-SiC DMOSFETs, are given on the same diagrams. Values of the used parameters are: gate to source voltage V_{GS}=16V, doping concentration N_a=10^{20}m^{-3}, temperature T=300K (Fig. 3) and T=600 K (Fig. 4). Under the same conditions, 3C-SiC DMOSFET drain current is the highest, 6H-SiC DMOSFET current follows and 4H-SiC DMOSFET current is the lower. This is not just consequent ion of different threshold voltage V_T, but also is consequent ion of different carrier's mobility in different polytypes (see Table 1). The differences in the drain current are of course bigger for the higher gate voltage.

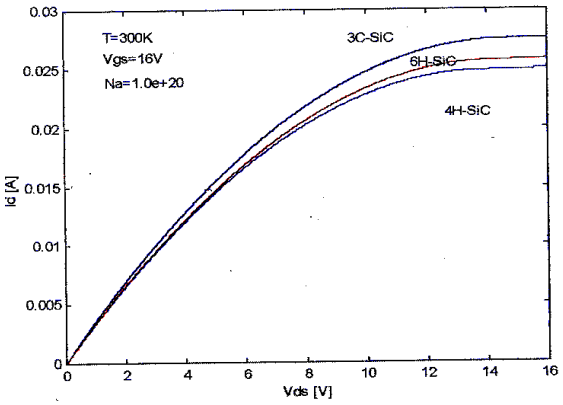

Fig. 3. 3C, 4H, 6H-SiC DMOSFET output characteristics, on the room temperature, V_{GS}=16V, N_a=10^{20}m^{-3}.

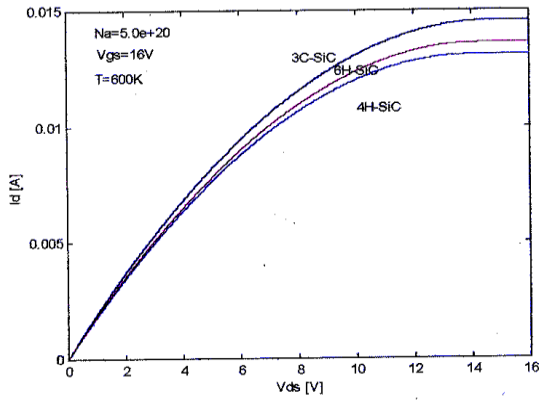

Fig. 4. 3C, 4H, 6H-SiC DMOSFET output characteristics, $N_a = 5\times10^{20}\ m^{-3}$, $V_{GS} = 16$ V, $T = 600$ K.

4. Conclusions

In this paper analytical model of drift region voltage, in vertical SiC DIMOSFET, is developed. Region of interest is devided into three segments – channel and two zones: accumulation zone and drift zone; voltage anlytical model for each zone is developed. Channel voltage is separately taken into account. This division directly coresponds to transistor behaviour and describes physical processes very realistically. Consequently, proposed model is accurate, because it is based on transistors physics. At the same time, exposed model is relatively simple, thus it can easily be used. The model is modular and thus it can easily be tested, upgraded and eventualy changed. To verify the developed drain to source voltage model, it is incorporate into the I-V characteristics model and simulations were performed. Obtained results are in very good agreement with the ones available in literature.

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