An implementation of area and power efficient digital FIR filter for hearing aid applications

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Very Large Scale Integration (VLSI) implementations specifically for low power, area efficient, and Energy delay product in TSMC 90nm technology to test the necessity of giving 100% usefulness of the harmed human hearing devices. The linear phase finite impulse response (LPFIR) filter is utilized for low area and less power consumption. In LPFIR filter, the logic optimization relies on the accessibility of redundant operations in the detailing. However, multiplication and accumulation path logic optimized without giving any thought to the data dependence. The proposed digital FIR filter logic is dispensed all of the redundant logic operations of the LPFIR filter and logic optimized in the data dependence. Wallace tree multiplier, carry save multiplier, transmission gates multiplier, ripple carry multiplier and booth carry save multiplier also been approached for hearing aid. But Hybrid multiplier with modified conventional carry save adder is proposed in digital FIR filtering architecture. An area efficient and power consumed reconfigurable non-uniform computerized programmed digital finite impulse response (FIR) filter is utilized in the hearing aid application. The digital FIR filter is implemented in TSMC 90nm technology. The proposed multiplier gets less 285 logic cells, 1087 numbers of logic equivalents, 28000 μm^2 area, 2.7W/Hz dynamic energy, 0.39nw static power, 95ns delay and 0.26Js energy delay product. The proposed method is covered 36798 logic gates and consumed 75.4μw power with 182.5ns delay.

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1. Introduction

A hearing aid [1-4] is an electro acoustic gadget which is intended to increase sound for the wearer, typically to the point of making discourse more comprehensible, and to amend impeded hearing as measured by an audiometer. In the U.S, Hearing supports are viewed as restorative gadgets and are directed by the Food and Drug Administration (FDA). Common little sound speakers or other plain sound strengthening frameworks can't be sold as "portable amplifiers".

The main hearing aids [3, 5-7] were ear trumpets, and were made in the seventeenth century. A portion of the first hearing aids were outer hearing aids. Outside hearing devices steered sounds before the ears and hindered all other noises. The mechanical assembly would fit in the back or in the ear. The development of advanced hearing aids started with the formation of the phone, and the first electric hearing aid was made in 1898. By the late twentieth century, computerized hearing aid amplifiers were economically accessible. The development of the carbon microphone receiver, transmitters, computerized sign handling chip, and the improvement of machine innovation helped change the portable hearing aid in its available form.

The main electrical hearing aid device utilized the carbon microphone of the phone and was presented in 1896. The vacuum tube made electronic enhancement conceivable, however early forms of intensified portable hearing aids were so substantial there was no option bear. The transistor concocted in 1948 was appropriate to the hearing aid device application because of low power and little size; portable hearing aid amplifiers were an early adopter of transistors. The improvement of incorporating circuits permitted further change of the capacities of wearable aids, including execution of computerized sign transforming procedures and programmability for the individual client's requirements. Hearing aid amplifiers are one of numerous modern, versatile, computerized frameworks obliging power efficient plan to drag out the battery life. Hearing aid amplifiers perform signal transforming capacities on audio signals. With the approach of numerous new signal transforming techniques, their prerequisite for higher computational capacity has put extra weight on power consumption. Hearing aid devices [8,9] are a common sample of a compact device. They incorporate computerized signal preparing algorithms, which request extensive processing power. Yet, smaller than expected pill estimated batteries store a little measure of vitality, constraining their lifetime. Hence, it is obligatory to utilize low-power outline and circuit strategies without ignoring their effect on zone occupation. Hearing impairment has frequently gone hand in hand with diminished recurrence selectivity which prompts diminished discourse coherence in noisy situations.

One probability to assuage this insufficiency is the phantom honing for speech enhancement taking into account adaptive filtering [10-12]; the imperative frequency commitments for understandability in the speech are distinguished and accentuated. Due to territory area constraints, such algorithms are generally executed in completely time-multiplexed architectures, in which different operations are booked to run on a couple of processing units. Ripple carry multiplier [13] and carry save multiplier [14] differed in carry propagation. In ripple carry multiplier, the carry bits are moved from right to left. The carry save multiplier is executed with booth encoding and added it one descend row. Wallace tree multiplier is added all partial product terms in final adder. This work [15] talks the area and power utilization and implementation of the discourse speech enhancement algorithm. Hence, low power and area efficient hybrid booth dadda multiplier is utilizing in digital FIR filtering process for hearing aids. We explore the utilization of multipliers for transforming audio signals. Through correlation, we demonstrate how the area and power consumption can be brought down for audio signal processing utilizing tweaked multiplier and modified conventional carry save adder while keeping up the general signal quality. In section II, discussing about the multi channel hearing aid signal processing, in section III, describing of digital filter, section IV discusses about the result and section V concludes the paper.

2. Multi-channel hearing aid signal processing

Linear amplification with gradually adjusting programmed gain control currently as of now overwhelms propelled portable hearing aid design, and has been widely considered [10-11]. The ordinary cochlea, on the other hand, utilizes non-linear, quickly compressive enhancement under efferent control, whose striking attributes have been demonstrated and are mulled over efficiently for utilization in multi-channel amplifiers [12]. Basically, we are endeavoring to copy the critical parts of a healthy ear to guide the outline of future listening hearing aids. A block diagram of the obliged processing signal is shown in Fig. 1.

Fig. 1 demonstrates the piece outline of generic hearing aid, sound-related compensation, echo abrogation, noise lessening/concealment, speech enhancement and so on. Sound-related compensation is the fundamental function in hearing aids, which performs a recurrence shaping to compensate for the listening to misfortune hearing loss. An individual filter channel in the filter bank decays the input signal into uniform recurrence or non-uniform recurrence frequency bands. A low pass filter outputs the most minimal frequencies, a high pass filter outputs the most noteworthy frequencies and a set of band pass filters output the staying middle of the frequencies as shown in Fig. 1, with the goal that the endorsed gain focused around the audiogram or hearing threshold can be connected to the distinctive frequency bands to suit the needs of the listening to impeded individuals, or in other words the adequacy response of the filter bank ought to equalize the audiogram.

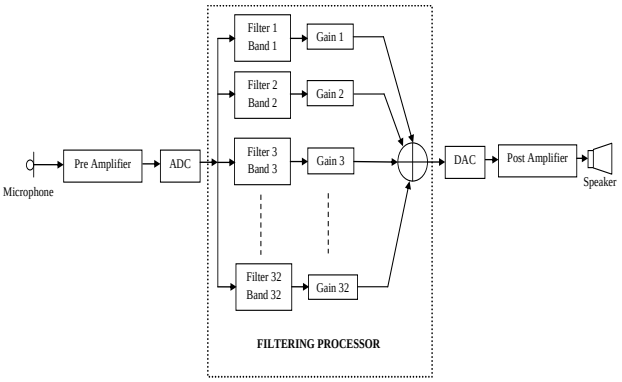

Fig. 1. Block diagram of multi-channel hearing aid signal processing [1].

The greater part of the present accessible hearing aid device outlines give the filter bank with uniform recurrences or non-uniform recurrences. Hence the patients can't take the full lead to enhance their particular auditive performance execution by utilizing the hearing aid with restricted number of fixed bands. This decreases the potential adaptability in matching of hearing to misfortune with steeply slanting audiograms. One technique of enhancing the same is to utilize an instrument with higher number of frequency recurrence bands for matching the audiogram with least error. At the same time such a usage would not just oblige a large amount of processing power additionally increases the expense cost. Modern portable hearing aid devices with 32 bands are extremely helpful to design a filter structure and that can be effortlessly customized with least change in parameters, for any hearing to disabled person.

3. Digital filter architecture

Over a scope of uses, the most normal function executed in the elite performance signal processing is a finite impulse response (FIR) filters. The digital signal processing (DSP) design must be enhanced; and to permit the most productive implementation of DSP structures as this straightforwardly deciphers into cost and power. Fig. 2 demonstrates an FIR filter architecture, which obliges multipliers, registers, and adders for its usage. The FIR filter structure can implement the registers, hybrid multipliers and modified conventional carry save adders to the variable accuracy in a single DSP block. An alternate basic implementation of the FIR filter is the systolic FIR filter. In this FIR filter, the architecture design is done addition in an output systolic register after every adder stage. The variable accuracy of the DSP architecture design has such an output register incorporated with the DSP block.

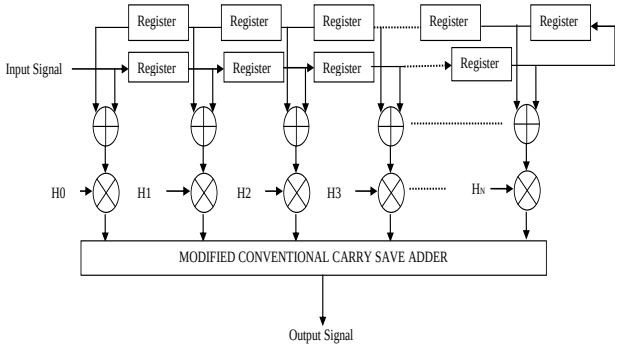

Fig. 2. FIR filter architecture.

3.1 Hybrid multiplier

To produce multiply X by Y utilizing the adjusted Booth calculation begins with gathering Y by three bits and encoding into {-2, -1, 0, 1, 2} coefficients. Table 1 demonstrates the standards to create the encoded signals by BE plan and Fig. 3 (a) demonstrates the relating logic diagram. The Booth decoder creates the partial products utilizing the encoded signals as demonstrated in Fig. 3(b).

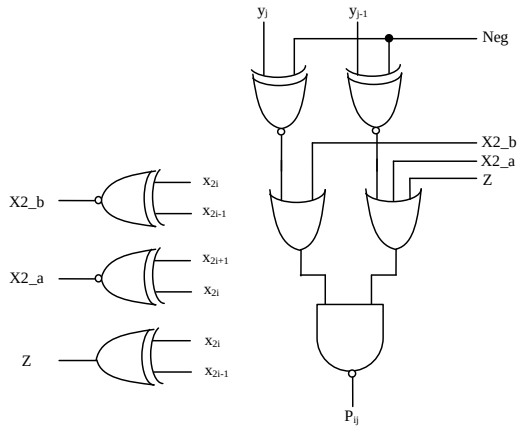

Fig. 3. (a) Simple Booth encoder (b) Decoder.

The Booth Encoding recorder was composed by emulating investigation. Table 1 displays the reality of the encoding method. The Z signal makes the output zero to repay the inaccurate $X2\_b$ and Neg signals. Fig. 3 introduces the circuit outline of the encoder and decoder of Booth Encoding. The encoder produces X_{1_a}, X_{2_b}, and Z signals by encoding the three x signals. The y low significant bit (LSB) signal and is consolidated with x-signals to focus the row LSB and the Neg_cin signals. Essentially, yMSB is consolidated with x- signals to focus the sign expansion signals. Fig. 4 demonstrates the partial product and sign expansion method of the 8 bit changed the Booth multiplier. The partial products produced by the adjusted Booth calculation are included in parallel utilizing the dadda tree. The final multiplication results are created by including the last rows. The modified carry propagation adder is generally utilized as a part of this step.

Table 1. Booth encoder truth table.

b_{i+1}	b_i	b_{i-1}	Value	X_{1_a}	X_{2_b}	Z	Neg
0	0	0	0	1	0	1	0
0	0	1	1	0	1	1	0
0	1	0	1	0	1	0	0
0	1	1	2	1	0	0	0
1	0	0	-2	1	0	0	1
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1	1	0	-1	0	1	1	1
1	1	1	0	1	0	1	1

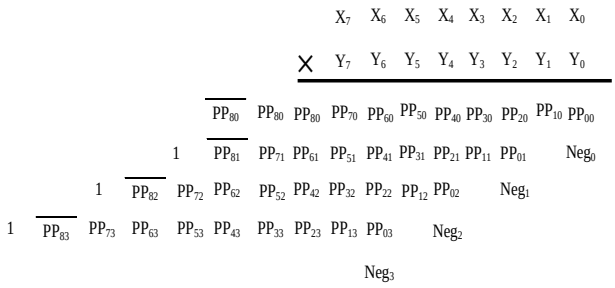

Fig. 4. Created partial products and sign expansion method.

Dadda summed up and augmented Wallace's results by noting that a full adder can be considered as a circuit, which includes the no. of ones in the inputs-outputs, that number in 2-bit binary structure. Utilizing such a counter, Dadda hypothesized that, at each one stage, just least amount of reduction ought to be carried out with a specific end goal to diminish the partial product matrix by a component of 1.5. However Dadda's method does the minimum lessening fundamental at each one level as that of Wallace method. This results in an outline with less number of logic gates in adders.

3.2 Modified conventional carry save adder

A conventional carry save adder (CSA) is a ripple carry adder (RCA) arrangement that produces a couple of sum and carry. An ordinary CSA has less carry propagation delay than an RCA, yet the outline is not alluring since it utilizes RCA. In the proposed adder, the carry operation is planned before the calculation of final-sum, which is not the same as the conventional methodology. Settled input bits of the carry generator unit are likewise utilized for logic optimization. Fig. 5 demonstrates the modified conventional carry save adder. In light of this, an enhanced configuration of carry generation units is obtained. Utilizing these improved logic units, an efficient configuration is acquired for the adder. The proposed adder design fundamentally occupies less area and less delay than the regular adder. This proposed adder eliminated all the redundant logic operations of the original carry save adder. In the proposed scheme, the Carry operation is programmed earlier than

the computation of final-sum, which is diverse from the usual approach.

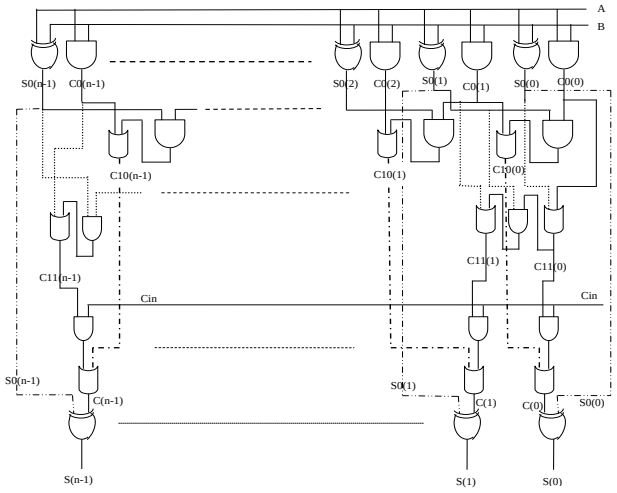

Fig. 5. Modified Conventional Carry Save Adder design, where n is the input operand bit-width.

4. Results and discussion

The greater part of the present accessible hearing aid device outlines give the filter bank with uniform recurrences or non-uniform recurrences. The Digital FIR filter is executed by using Verilog HDL. The DSP design must be enhanced to permit the most productive implementation of these structures as this straightforwardly deciphers into cost and power. The Table 2 compared proposed method with LPFIR filter in number of no. of logic gates, delay, Frequency, and power usage. The digital FIR filter is implemented in TSMC 90nm technology. The digital FIR filter is covered 35798 logic gates and consumed power (75.4μw) with delay (82.5ns).

Table 2. Proposed method final report comparison with existing.

	LPFIR [13]	Proposed
Area in gates	37542	36798
Delay (ns)	80.2	182.5
Frequency (MHz)	92.81	54.8
Power (μw)	80.6	75.4

The proposed multiplier is compared with different types of multiplication methods in number of logic cells, number of gate equivalents, dynamic energy, static power, delay and energy delay products, shown in Table 3, and Fig. 6 shows the comparisons in charts. Cells count: As compared with other techniques, the proposed multiplier gets less number of logic cells (285) and booth carry save multiplier gets more logic cells (663).

Gate Equivalent: Proposed multiplier gets 1087 numbers of logic equivalents, whereas RCM gets 2053 number of logic equivalents.

Area: Proposed multiplier (28000 μm^2) is very good area efficient as compared with the Ripple carry multiplier (RCM), Carry save multiplier (CSM), Wallace tree multiplier (WTM) Booth carry save multiplier (BCSM) and Transmission gates multiplier (TGM). RCM and WTM occupied same area (43000 μm^2), and BCSM occupies more area (45000 μm^2).

Dynamic Energy and Power: The proposed multiplier consumes less dynamic energy (2.7W/Hz) and static power (0.39nw), RCM consumes more dynamic energy (14.6W/Hz), and booth carry save multiplier consumes more leakage of static power (1.08 nw).

Delay: Proposed multiplier of the Partial product generation process has taken more time (95ns) to execute. This is the main disadvantage of the proposed multiplier. The WTM has shortest delay (91ns) and RCM has the longest delay (234ns).

Energy delay product: Due to the less consumption of power as compared with other multiplier techniques, the proposed multiplier gets less energy delay product (0.26Js). RCM gets more energy delay product (3.42Js).

Table 3. Comparison in terms of No. of cells, No. of GEs, area on silicon, Dynamic energy, Static power, Delay of RCM, CSM, WTM, BM, TGM and proposed multiplier.

	Ripple Carry Multiplier (RCM)	Carry Save Multiplier (CSM)	Wallace Tree Multiplier (WTM)	Booth- carry save Multiplier (BCSM)	Transmission Gates Multiplier (TGM)	Proposed Multiplier
No. of logic cells	512	497	531	663	-	285
No. of Gate Equivalents	2053	2000	2045	2037	-	1087
Area in μm^2	43000	42000	43000	45000	41000	28000
Dynamic Energy [lW/MHz]	14.6	10.9	6.0	11.0	3.1	2.7
Static Power in nW	0.88	0.84	0.94	1.08	0.55	0.39
Delay in ns	234	142	91	125	223	95
Energy Delay Product (J.S)	3.42	1.55	0.55	1.38	0.69	0.26

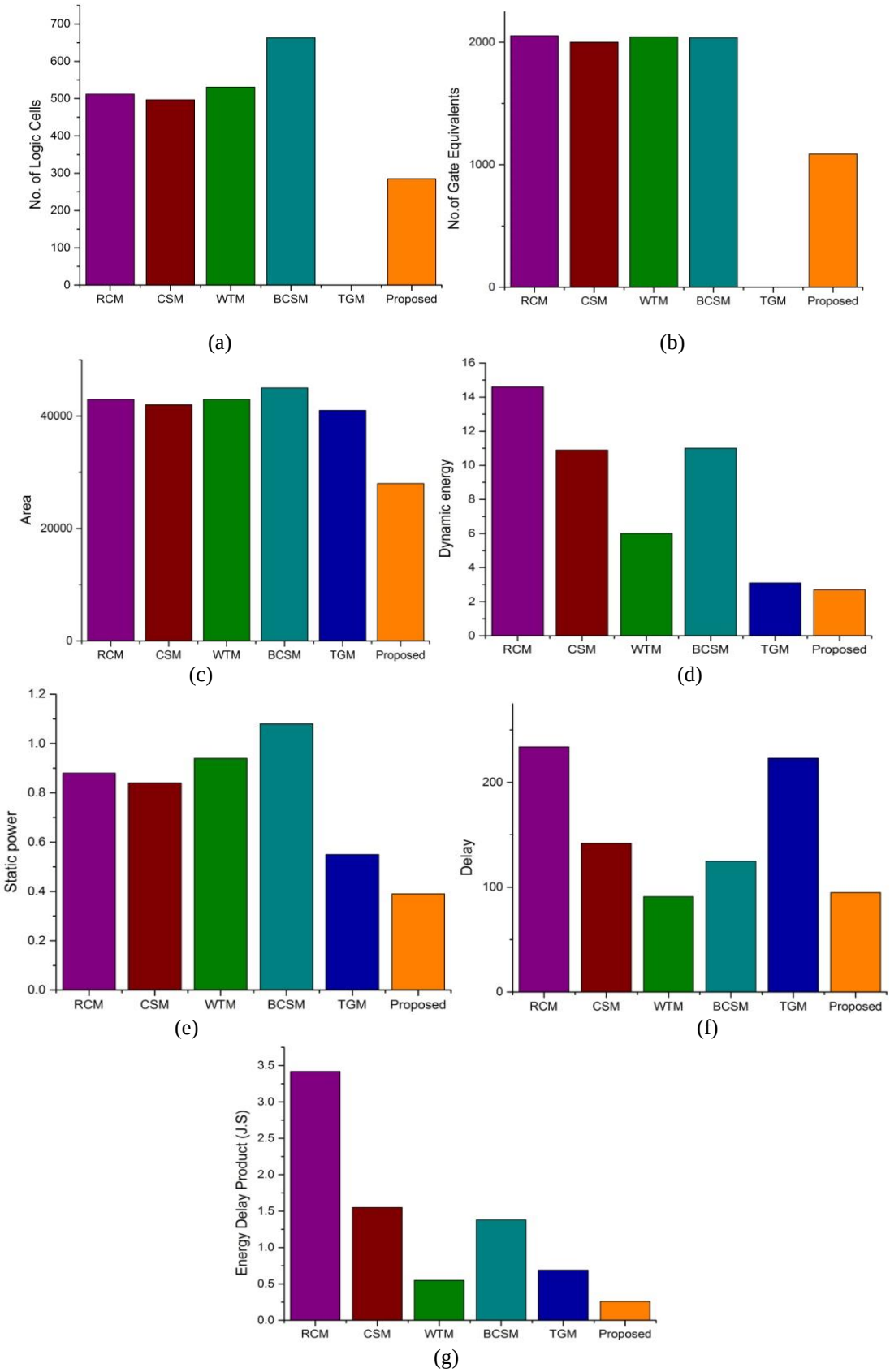

Fig. 6. The proposed multiplier is compared with different types of multiplication methods in (a) number of logic cells (b) number of gate equivalents (c) Area in μm^2 (d) Dynamic Energy (e) static power in nW (f) delay in ns (g) Energy Delay Products in JS.

5. Conclusion

The hearing aid device relies on the analysis parameters and synthesis filters and additionally on the number of stages taken to execute the outline design. A hearing aid component is executed and assessed. The hearing aid channel amplifier is also developed. The implementation is done in the filtering process. The FIR filter is indicated to save huge area, power and delay. However, multiplication and accumulation path logic optimized without giving any thought to the data dependence. The proposed digital FIR filter logic is dispensed all of the redundant logic operations of the LPFIR filter and logic optimized in the data dependence. Despite the fact that the particular results presented for hearing aid component in Verilog HDL sector restricted to a solitary stage, utilizing the results of single stage hearing aid in Verilog HDL. The digital FIR filter is implemented in TSMC 90nm technology. The proposed multiplier gets less 285 logic cells, 1087 numbers of logic equivalents, 28000 μm^2 area, 2.7W/Hz dynamic energy, 0.39nw static power, 95ns delay and 0.26Js energy delay product. The proposed method is covered 36798 logic gates and consumed 75.4μw power with 182.5ns delay.

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