

Characterization of series resistance in the Sn/p-InP Schottky barrier diodes using temperature dependent C-V, G/w and DLTS

D. KORUCU*, Ş. ALTINDAL, T. S. MAMMADOV^a, S. ÖZÇELİK

Physics Department, Faculty of Arts and Sciences, Gazi University, 06500, Ankara, Turkey

^a*National Academy of Science, Institute of Physics, Baku, Azerbaijan*

The temperature dependence of capacitance-voltage (C-V) and conductance-voltage (G/w-V) characteristics and DLTS measurements of Sn/p-InP Schottky barrier diode (SBDs) have been investigated in the temperature range of 80-400 K at 1 MHz. Experimental results show that both the C-V and Rs-V plots exhibit a peak, and this peak positions shift toward positive bias voltage with increasing temperature. The C-V and G/w-V characteristics show that the interface states (N_{ss}) and series resistance (R_s) are strongly influence the electrical parameters of the Sn/p-InP (SBD). Also, Deep level transient spectroscopy (DLTS) measurement has been performed to investigate defects in bulk p-type InP doped with Zn.

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1. Introduction

Indium Phosphide (InP) is a promising substance for high speed digital, optoelectronic and microware application [1,2]. Also it can be used for the fabrication of solar cells, radiation detector and semiconductor lasers [3] too. But one of the drawback factors in the reliability and performance of InP based devices is the existence of deep levels in the energy band gap of the semiconductor. These defects study in InP is very important. Therefore, the characterization and control of the energy distribution of deep levels and their cross sections for electron capture are important problems in semiconductors technology [4]. The changes in temperature and bias voltage have important effect on the electrical parameters such as barrier height (BH) between metal and semiconductor (M/S), R_s of devices, the N_{ss} between semiconductor and insulator of metal-semiconductor (MS) SBD. An anomalous peak in the forward bias C-V characteristics has reported before [5-7].

The origin of this anomalous peak is attributed to the N_{ss} [8] and Werner et al. [9] have shown that the observed peak in the forward bias (C-V) characteristics is due to R_s of device. Also, the influence of defects on the electronic and optical properties of semiconductor materials is known to be significant. DLTS is a powerful technique to investigate defects in semiconductors and this method is used to find characteristics trap parameters such as activation energies (E_a), capture-cross section (σ) and concentration (N_T) [10-11].

DLTS technique employs a reverse biased junction which is pulsed electronically to inject majority carrier. For a pulse of suitable duration the injected carriers will fill traps in the InP bandgap. After the filling pulse with

fill pulse length the traps will be empty. The temperature dependent of capacitance transient can be recorded as a DLTS spectrum [12].

In this study, the experimentally C-V and G/w-V characteristics of Sn/p-InP SBDs have been investigated by considering the N_{ss} and R_s effects in the wide temperature range (80-400 K). For the DLTS measurements, using a Sula Technology compact system have been used at constant reverse bias with suitable value of filling pulse at the same temperature range.

2. Experimental procedure

Cleaning and contact procedure detail of Sn/p-InP SBD were published in another paper [13-14]. The capacitance-voltage-temperature (C-V-T) and conductance-voltage-temperature (G/w-V-T) characteristics of fabricated Sn/p-InP Schottky barrier diodes (SBDs) were measured in the temperature range of 80-400 K at 1 MHz. The C-V and G/w-V measurements were performed at 1 MHz by using HP 4192A LF impedance analyzer (5 Hz–13 MHz) and the test signal of 40 mV_{rms}, using a temperature controlled Janes vpf-475 cryostat. The sample temperature was measuring with a dmm/scanner Keithley model 199 and a Lake Shore model 321 auto-tuning temperature controllers. Investigation of deep level in Sn/p-InP SBD, a Sula Technologies DLTS system have been used in the same temperature range at the chosen emission rates, reverse bias voltage with suitable fill pulse and fill pulse length.

3. Results and discussion

In this study, Nicollian and Goetzberger method for calculation of series resistance was used and given Eq. (1). In this equation, C_m and G_m/w are the measured capacitance and conductance for any bias voltage at high frequencies ($f \geq 1$ MHz), respectively [15],

$$R_s = \frac{G_m}{G_m^2 + (\omega C_m)^2} \quad (1)$$

Temperature dependence of C - V , G/w - V characteristics of Sn/p-InP SBD have been measured at the temperature range of 80-400 K and were given in Fig. 1(a) and (b), respectively. As seen in Fig. 1(a), the values of C give a peak in each temperature, shifting to reverse bias region with increasing temperature. Also, it is clear that from the Fig. 1(a), the change in the temperature has effects on the values and positions of these anomalous peaks of capacitance. Fig. 1(b) shows G/w - V characteristics of the SBD and the value of G/w increases with increasing temperature especially at low bias voltage. The series resistance is calculated according to Eq. (1) and shown in Fig. 2 for various temperatures.

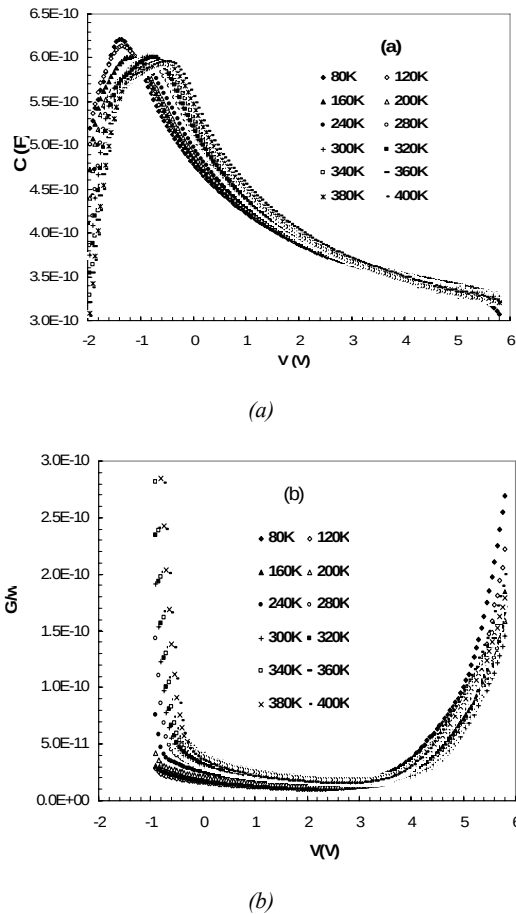


Fig. 1. (a) The capacitance-voltage (C - V - T) and (b) conductance-voltage (G/w - V - T) characteristics of Sn/p-InP SBD at 1 MHz.

As seen in Fig. 2 (a), the series resistance gives a peak in the reverse voltage range depending on temperature. It is clearly seen in Fig. 2 (a) that the series resistance is independent of voltage at around the forward bias region. In addition the temperature dependence of the R_s for various forward bias voltages can be seen in Fig. 2 (b). It shows that the R_s values are voltage dependent and increase with increasing temperature until 350 K after that give a peak. Also the capacitance values are independent temperature, especially at low temperature.

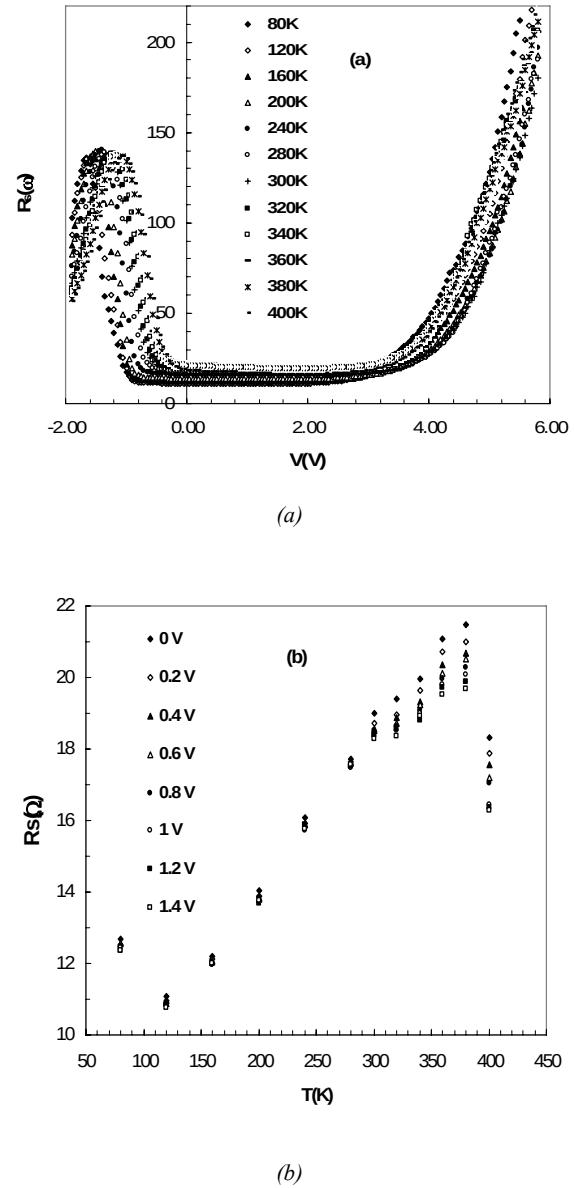


Fig. 2. (a) The variation of the series resistance of Sn/p-InP SBD as a function of voltage for various temperature and (b) The variation of R_s as a function of temperature for various voltages ranged from 0 V to 1.4 V at the same structure at 1MHz.

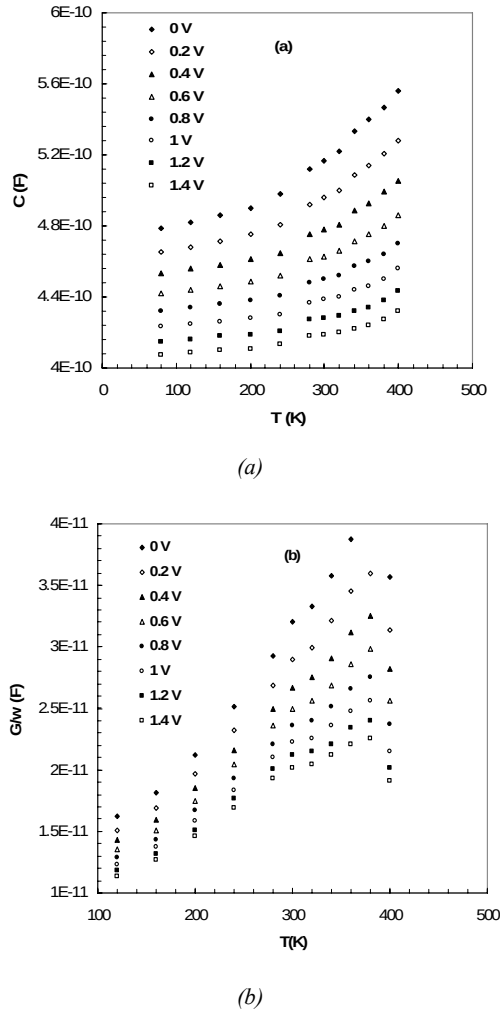


Fig. 3. The temperature dependence of the experimental (a) C-V and (b) G/W-V characteristics of the Sn/p-InP SBD for various voltage values ranged from 0 V to 1.4 V.

Fig. 3 (a) and (b) show the voltage dependent of the capacitance C and conductance G/W measurement in studied temperature range. As shown in Fig. 3 (a), C values usually increase with increasing temperatures, especially high temperature region for each bias voltage. On the other hand, G/w values (Fig. 2 (b)) increase with increasing temperature and then give a peak about after room temperature. We considered that the trap charges have enough energy to escape from the traps located between metal and semiconductor interface in the InP band gap.

The trap decay process is recorded as a function of temperature in DLTS measurement. The emission rate in DLTS is written by

$$e = \frac{N_0 \sigma V_{th}}{g} \exp\left(-\frac{E_a}{kT}\right) \quad (2)$$

where N_0 is the effective density of states, σ is the capture cross-section, V_{th} is the thermal velocity and g is the

degeneracy of the level ($g=2$). If σ is independent of temperature, the activation energy E_a shows the energy of the trap from the band edge to which carriers are emitted. E_a can be obtained from the slope of $\ln(e/T^2)$ - $1/T$ plot and the capture cross-section can be calculated from intercept of Arrhenius plot. In our previous study, we have reported DLTS spectrum in MBA grown epilayer n-InP SBD[16].

Defect concentration is obtained from the peak height and is written as

$$N_T = \frac{2\Delta C}{C} (N_D) \quad (3)$$

where ΔC is the capacitance change, C is the capacitance of the diode under quiescent reverse-biased conditions, N_T trap concentration and N_D is the net donor concentration when the trap is seen. The reverse bias applied to the Schottky diode was at -1 V together forward filling pulse voltage was at 0.5 V with pulse widths 10 ms during the DLTS measurement. The temperature was swept at a rate of 0.2 K/s and the measurements have been performed for various rate windows between 5ms and 0.5 ms. One trap level has been observed in DLTS spectrum (Fig 4. (a)). Trap activation energy and capture cross section have been calculated from Arrhenius plot (Fig. 4 (b)) as a 0.31 eV, $7.22 \times 10^{-19} \text{ cm}^2$, respectively. Also trap concentration is calculated from Eq. (3) as a $4.51 \times 10^{15} \text{ cm}^{-3}$. The experimental results of DLTS show that defects with energies in the region of $E_v + 0.30 \text{ eV}$ are due to some Zn-related configuration [17,18] in the LEC grown material p -type InP.

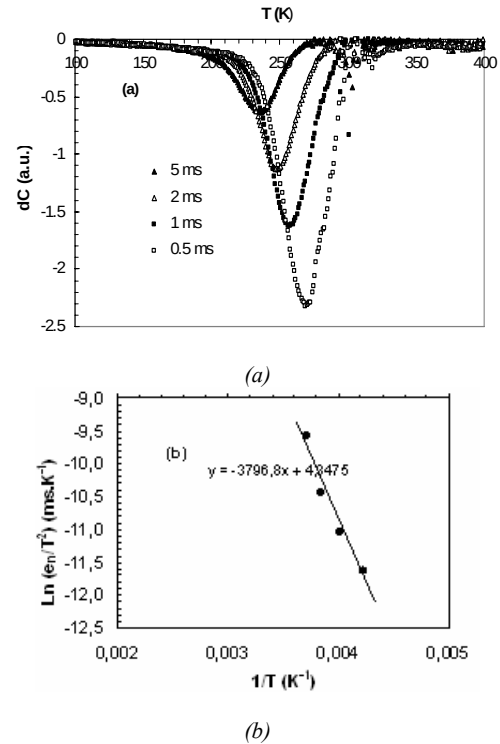


Fig. 4. (a) DLTS spectrum in p -type Sn/p-InP SBD. (b) Arrhenius plot obtained from DLTS spectrum.

4. Conclusions

To investigate the effects of N_{ss} and R_s of Sn/*p*-InP SBDs, the forward C - V and G/ω - V characteristics have been measured in the wide temperature range of 80-400 K. Experimental results show that both the both C - V and R_s - V plots exhibit an anomalous peak and these peaks positions shift toward positive bias voltage with increasing temperature. From the DLTS spectrum, one peak has been observed with energy in the region around $E_v + 0.30$ eV. This trap level can be ascribed to Zn related defect in the LEC grown *p*-type InP.

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*Corresponding author: dkorucu@yahoo.com